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INSTRUCTION MANUAL

MODEL 172B PROGRAMMABLE SIGNAL SOURCE

WAVETEK

WAVETEK SAN DIEGO, INC.

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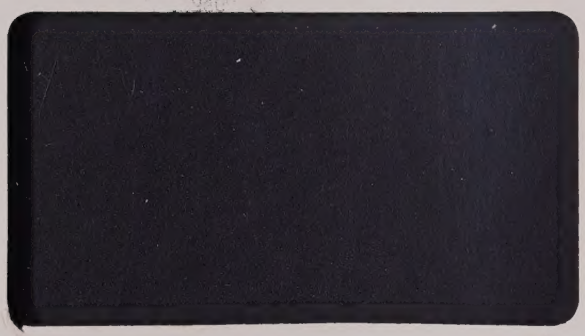

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MODEL 172B PROGRAMMABLE SIGNAL SOURCE

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

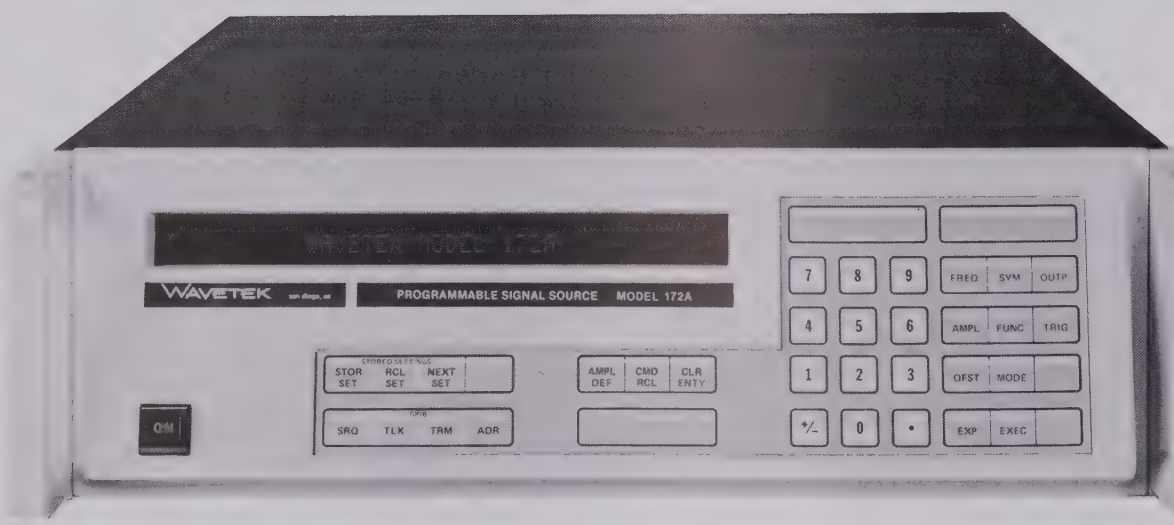
BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.



Model 172B Programmable Signal Source

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 172B AND OPTIONS

1.1.1 Standard Model

The standard Model 172B is a remote controlled 0.1 mHz to 13 MHz function generator whose functions are sine, square, triangle, pulse, ramps, haversine, havertriangle (see figure 1-1) and dc with 3 digit frequency, amplitude and dc offset amplitude resolution. Frequency, amplitude, function, function symmetry, dc offset, mode, 50Ω load in/out and output on/off are programmable. The frequency may also be controlled by a remote ac or dc voltage for sweep, FM and frequency shift keying operations. The output frequency of the generator may be phase locked to a supplied reference signal for a phase coherent output signal. The generator output may be continuous, triggered for one cycle (by external signal keyboard or program) or gated for a burst of cycles by an external signal. The output signal may be offset by a dc voltage or inverted 180 degrees. The waveform symmetry may be varied from 10 to 90% in 10% steps for variable duty cycle pulses, sawtooth ramps and non-symmetrical sine waves. A TTL level signal at generator frequency is output for synchronizing purposes. Standard programming is by a General Purpose Interface Bus (GPIB) conforming to IEEE Standard 488-1975, which utilizes an asynchronous handshake scheme to transmit an 8-bit parallel, byte serial ASCII language data stream. A stored program feature allows temporary storage of up to 240 instrument settings by use of Random Access Memory (RAM). Rapid setting recall allows frequency sweeps. An amplitude conversion feature allows sine wave amplitude programming in convenient dBm and rms values, as well as volts peak-to-peak into a 50Ω load.

1.1.2 Front Panel Option

The front panel option, an instrument mounted keyboard and 40 character display, gives local control of the instrument. The display shows the values being programmed and the status of the instrument parameters when in either local or remote control.

1.1.3 Synthesizer Option

The synthesizer option provides 5½ digit frequency resolution with 0.0005% accuracy, low phase noise and low spurious content. The internal 10 MHz reference is also output as a TTL pulse for synchronous operation. An external 10 MHz reference may be substituted for the internal reference.

1.2 SPECIFICATIONS

1.2.1 Versatility

Waveforms

Sine , square , triangle , pulse , , ramps , , haversine , havertriangle and dc.

Operational Modes

Synthesizer: A closed loop mode locking the generator to a synthesizer for frequency accuracy and stability. See Option 002.

Phase Lock: Generator locks to an external 10 Hz to 13 MHz signal when programmed within 2% of the external frequency.

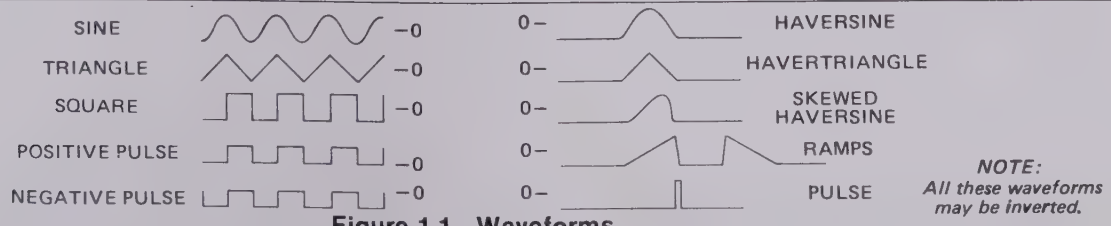


Figure 1-1. Waveforms

NOTE

The following modes are open loop; frequency of generator is not locked to a reference signal. Generator frequency is controlled by external VCG or FM voltage as well as programming.

Continuous: Generator runs continuously.

Triggered: Generator is quiescent until triggered by an external signal or manual trigger, then generates one cycle at selected frequency.

Gated: As triggered mode, except generator oscillates for the duration of the gate signal plus the remainder of the waveform in progress.

Triggered Haverwave: As triggered mode, except output is a sine or triangle waveform starting at −90° (or +90°).

Gated Haverwave: As gated mode, except output is a sine or triangle waveform starting at −90° (or +90°).

Frequency Range
0.0001 Hz to 12.99 MHz.

Resolution
3 digit resolution standard. Also see Option 002.

Main Output
∿, ⊓, ∿, ◿, ◺, ⩘, ⩔ and dc variable to 30V p-p (15V p-p into 50Ω load) with 3 digit resolution. ⎍ and ⎌ variable to ±15V p-p (7.5V p-p into 50Ω load) with 3 digit resolution. Composite waveform/offset not to exceed ±7.5V peak into 50Ω load. 50Ω source impedance with selectable internal 50Ω load.

Amplitude Output Conversion
Permits programming of the sine wave output amplitude in units of volts - root mean square (Vrms) and decibels relative to one milliwatt (dBm) into 50Ω load in addition to the standard units of volts peak-to-peak.
Vrms Range: 1 mV to 5.30V.
dBm Range: −56 to +27.4 dBm.

DC Offset and DC Voltage Output
0 to ±7.5 Vdc into 50Ω. 3 digit resolution. DC offset is attenuated by amplitude range attenuator.

Auxiliary Output
TTL pulse at generator frequency.

Phase Lock Input
Input: TTL level.
Range: 10 Hz to 13 MHz.

VCG - Voltage Controlled Generator
In open loop modes the frequency can be controlled by an external voltage for sweeping or for frequency modulation (FM). A 5V signal will change the frequency over the entire control range of 1000:1, three full decades. On ranges below 10 Hz, control is limited to 10:1.
Input Signal Bandwidth:
50 kHz for small signal (ΔV = 0.5V).
Input Impedance: 5 kΩ.

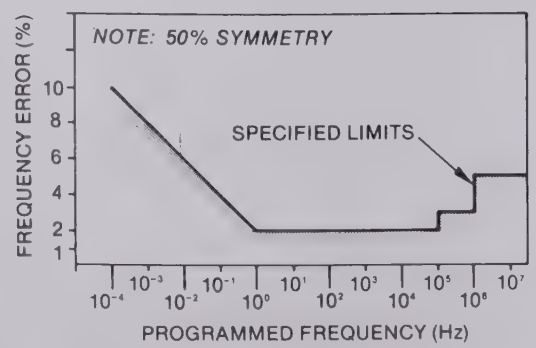
Symmetry Control
Waveform symmetry variable from 10 to 90% in 10% steps (50% is symmetrical). Varying symmetry provides variable duty cycle pulses, sawtooth ramps and unsymmetrical sine waves. Symmetry control is available for frequencies to 999,990 Hz.

Trigger Input
In triggered, gated, triggered haverwave and gated haverwave modes, a TTL (low true) compatible pulse will trigger or gate the generator.

Data Entry
Bit parallel, byte serial, ASCII character remote programming and optional front panel keyboard/display (see Option 001).

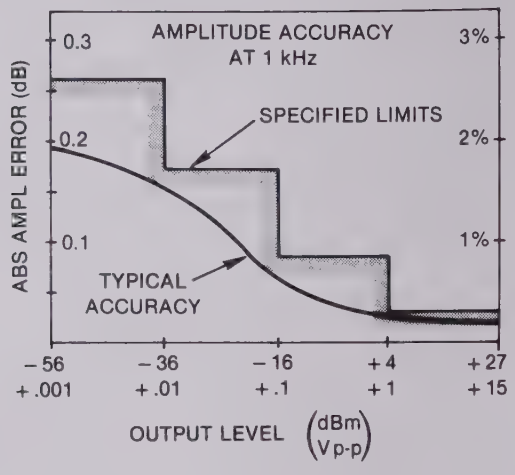
1.2.2 Frequency Precision

Open Loop Accuracy
(For synthesizer accuracy, see Option 002.)

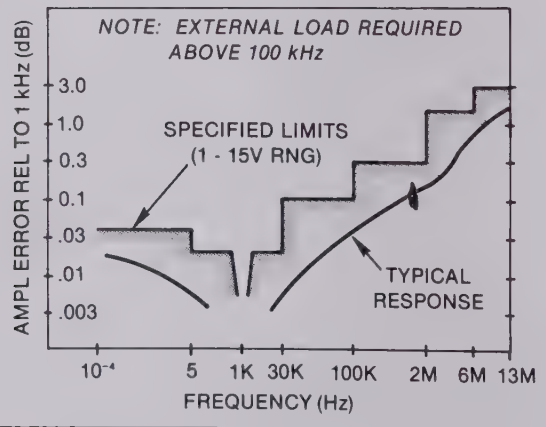


1.2.3 Amplitude Precision

Accuracy
Specified for 1 kHz sine wave or dc voltage output with internal 50Ω load and greater than 1 MΩ external impedance.



Frequency Response (sine wave, relative to 1 kHz signal)



NOTE

⎍ and ∿ accuracy are within 0.2 dB of sine wave accuracy.

Amplitude Resolution

Range	Resolution
10.00 to 14.99V	10 mV
1.00 to 9.99V	10 mV
100 to 999 mV	1 mV
10.0 to 99.9 mV	0.1 mV
1.00 to 9.99 mV	10 μV

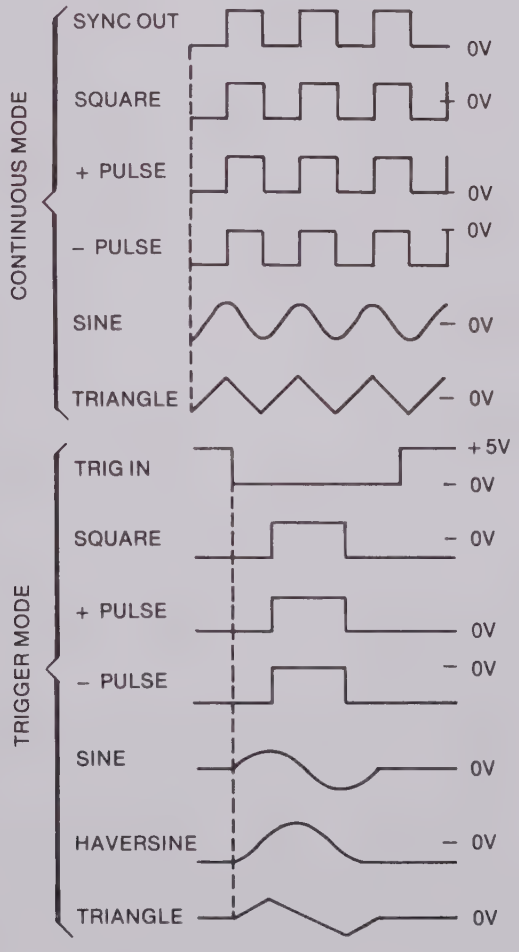
1.2.4 Waveform Characteristics

Sine Distortion
(continuous mode, 2.82V p-p test level)
Total harmonics referenced to carrier are −46 dB to 30 kHz. Each harmonic reference to carrier is less than:

−40 dB to 1 MHz
−30 dB to 13 MHz

Square Wave Rise and Fall Time
Less than 20 ns (typically 15 ns).

Waveform Timing



NOTE

Minus amplitude shifts all signals except sync by 180° and shifts baseline to opposite polarity.

GPIB Programming
General Purpose Interface Bus (GPIB) programming fully compatible with the IEEE Standard 488-1975 allows the 172B to be directly connected to the GPIB. The interface is isolated from the generator with optical couplers. The interface provides listener (AH1 and L4), talker (SH1 and T6), service request (SR1), remote/local (RL1), device clear (DC1) and device trigger (DT1) capabilities. Response time for setting and executing all parameters is 55 ms (18 settings per second); for setting and executing amplitude, frequency and dc offset, 39 ms (26 settings per second). A stored setting (all parameters) may be called by number and executed in 9 ms (111 settings per second); when using the GET command to sweep stored settings, response time is 2 ms (500 settings per second). The following table may be used to determine particular programming response times. Measurements were made with a 172B and an HP9825 controller. Data rates will follow the slowest listener on the bus and vary with different controllers.

Parameter	Time
Command Handshake	2 μs
Data Handshake	220 μs
Frequency Setting	10 ms
Amplitude Setting	13 ms
DC Offset Setting	13 ms
Mode	4 ms
Function	4 ms
Symmetry	4 ms
Output	4 ms
Recall Setting (by number)	6 ms*
Next or Last Setting	4 ms*
Execute	3 ms*
GET	1.6 ms

*2 ms when via GET.

Stored Settings and Sweep
Up to 240 complete instrument settings can be stored and recalled by number from volatile (RAM) memory. Settings may be modified or deleted. The setting number recalled may also be incremented or decremented and executed by the GET command, when in a special GET mode. This sweep stepping time requires 2 ms per setting.

1.2.5 General

Stability (measured at 25 ± 1°C)
Amplitude and DC Offset
Short Term: 0.025 dB for 15 minutes.
Long Term: 0.05 dB for 6 months.

Frequency
Short Term: 0.3% for 15 minutes.
Long Term: 1.0% for 8 hours (to 1 MHz).
See Option 002 for synthesizer stability.

Environmental
Specifications apply for 25 ± 10°C after 1 hour unless otherwise noted. Instrument will operate from 0 to 45°C to 10,000 foot altitude at 95% relative humidity.

Dimensions
Fits standard 48.3 cm (19 in.) rack. 43.2 cm (17 in.) wide; 13.3 cm (5¼ in.) high; 58.4 cm (23 in.) deep. Supplied with rack mount adapters.

Weight
26.3 kg (58 lb) net; 30.8 kg (68 lb) shipping.

Power
90 to 105V, 108 to 126V, 198 to 231V or 216 to 252V; 48 to 67 Hz; less than 200 watts.

1.2.6 Options

001: Display and Control Front Panel
This option includes a keyboard entry front panel and a 40 character alphanumeric display. The keyboard allows you to manually control all instrument parameters. The alphanumeric display indicates the values being programmed and also shows the status of the instrument when in the remote mode.

002: 5½ Digit Synthesizer
Provides synthesizer accuracy for any waveform selected. The following specifications apply.

Frequency
10 Hz to 12.9999 MHz.

Frequency Resolution

Range	Resolution
10 to 99.999 Hz	1 mHz
100 to 999.99 Hz	10 mHz
1 to 9.9999 kHz	0.1 Hz
10 to 99.999 kHz	1 Hz
100 to 999.99 kHz	10 Hz
1 to 9.9999 MHz	100 Hz
10 to 12.9999 MHz	100 Hz

Settling Time
Frequency reaches full accuracy 2 ms and 50 cycles after execution.

Accuracy

Better than 0.0005% of program setting (0.005% on 10-99 Hz range).

Frequency Stability

Short Term: $\pm 1 \times 10^{-7}$ of frequency per day.
Long Term: $\pm 1 \times 10^{-6}$ of frequency per month.
Temperature: 1.2×10^{-7} per °C.

Signal To Phase-Noise

Greater than 40 dB in a 30 kHz band centered on carrier but excluding a ±1 Hz band around the carrier.

Spurious

For spurious signals in the range of 400 Hz to 110 MHz, spurious levels are:

172B Frequency Range	Max Spurious Signals (greater value applies)
10 Hz to 999.99 kHz	−60 dB or 40 μV
1 kHz to 4.9999 MHz	−55 dB or 40 μV
5 to 12.9999 MHz	−50 dB or 40 μV

Internal Reference Output

10 MHz TTL compatible signal.

External Reference Input

An external sine or square wave within ±3 ppm of 10.0 MHz, 1 to 10V rms and 50 ±8% duty cycle will automatically replace the internal reference.

SECTION 2
INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

CAUTION

Do not mount this instrument by front panel alone. Slides or tray support is necessary to prevent instrument damage.

The generator can be used as a bench instrument or rack mounted. In either use, ensure that there is no impedance to air flow at any surface of the instrument. Before rack mounting, it may be desirable to perform the initial checkout (paragraph 2.2.5) to verify operation of all functions.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a 3 amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.

2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.

4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

Card Position	Input Vac	Fuse
100	90 to 105	3 amp
120	108 to 126	3 amp
220	198 to 231	1.5 amp
240	216 to 252	1.5 amp

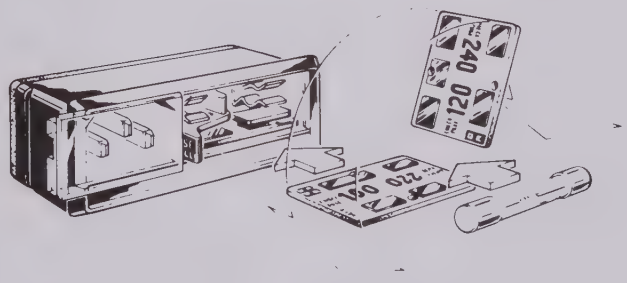


Figure 2-1. Voltage Selector and Fuse

2.2.2 Signal Connections

Use RG58U 50Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

2.2.3 GPIB Connections

The GPIB I/O rear panel connection is shown in figure 2-2; pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths). The GPIB interface is optically isolated from the instrument.

Table 2-1. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Safety Gnd	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Gnd
19		
20		
21		
22		
23		
24		

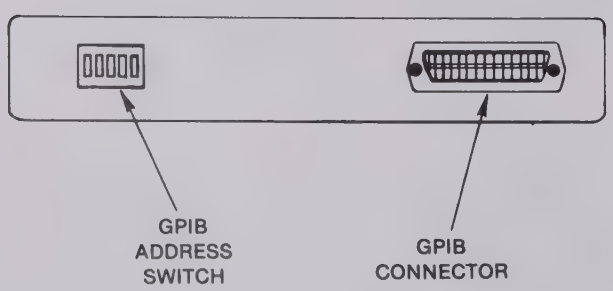


Figure 2-2. GPIB Panel

2.2.4 GPIB Card Address

For instruments on the General Purpose Interface Bus (GPIB), ensure that the GPIB address is correct. The GPIB address can be changed by the switch on the rear of the instrument (see figure 2-2) by simply setting the multiple section switch located on the rear panel according to table 2-2. The switch sections are labeled from 1 thru 5 and their open position noted (OPEN = Binary "0" in table 2-2). To verify the address, press ADR on the front panel. The device number (decimal) will be displayed as: "GPIB = (0, 1—30)".

Table 2-2. GPIB Address Codes

	Address								
	ASCII		Binary*					Hexa-decimal	
Device	Listen	Talk	5	4	3	2	1	Listen	Talk
0	(space)	@	0	0	0	0	0	20	40
1	!	A	0	0	0	0	1	21	41
2	"	B	0	0	0	1	0	22	42
3	#	C	0	0	0	1	1	23	43
4	$	D	0	0	1	0	0	24	44
5	%	E	0	0	1	0	1	25	45
6	&	F	0	0	1	1	0	26	46
7	'	G	0	0	1	1	1	27	47
8	(	H	0	1	0	0	0	28	48
9	)	I	0	1	0	0	1	29	49
10	*	J	0	1	0	1	0	2A	4A
11	+	K	0	1	0	1	1	2B	4B
12	,	L	0	1	1	0	0	2C	4C
13	—	M	0	1	1	0	1	2D	4D
14	•	N	0	1	1	1	0	2E	4E
15	/	O	0	1	1	1	1	2F	4F
16	0	P	1	0	0	0	0	30	50
17	1	Q	1	0	0	0	1	31	51
18	2	R	1	0	0	1	0	32	52
19	3	S	1	0	0	1	1	33	53
20	4	T	1	0	1	0	0	34	54
21	5	U	1	0	1	0	1	35	55
22	6	V	1	0	1	1	0	36	56
23	7	W	1	0	1	1	1	37	57
24	8	X	1	1	0	0	0	38	58
25	9	Y	1	1	0	0	1	39	59
26	:	Z	1	1	0	1	0	3A	5A
27	;	[	1	1	0	1	1	3B	5B
28	<	\	1	1	1	0	0	3C	5C
29	=	]	1	1	1	0	1	3D	5D
30	>	↑	1	1	1	1	0	3E	5E
			Switch Settings 0 = Open						

*The 6th and 7th bits which define the ASCII codes are used to specify whether a listen or talk address is being sent. Bits 1 thru 5 are matched against the rear panel address switch.

NOTE

Address 31 is not allowed.

2.2.5 Initial Checkout and Operation Verification

The equipment and procedures in tables 2-3 and 2-4 are recommended for incoming inspection and for testing the instrument after repair. However, additional after repair tests or calibation (Section 6) may be necessary for certain circuits.

Operation verification includes the following procedures.

1. Self Test: Verifies the operation of ROM, RAM and microprocessor circuits. This test occurs automatically each time power is turned on.
2. Open Loop Test: Sine wave output is visually checked for correct frequency and visible irregularities.
3. Functional Test: Verifies triangle and square waveforms.
4. Sync Out Test: Verifies presence of sync signal.
5. Amplitude Accuracy Test: Verifies amplitude accuracy for dc and ac operation.
6. Frequency Accuracy Test: Verifies frequency accuracy.
7. Harmonic Distortion Test: Verifies that harmonic distortion is with specification.
8. Spurious Test: Verifies that spurious are within specification.
9. Interface Test: Verifies remote programming capabilities.

Before making an initial checkout, review power and signal connection requirements (paragraphs 2.2.1 and 2.2.2) and ensure the availability of test equipment equivalent to that listed in table 2-3. An acceptance test record sheet (table 2.5) may be reproduced for recording checkout test results.

Table 2-3. Equipment Required for Incoming Inspection and Operation Verification

Instrument	Critical Specifications	Model Recommended
Oscilloscope	100 MHz vertical bandwidth	Tektronix 465
Voltmeter	0.1 to 10V ranges 6 digit resolution ±0.1% accuracy	Dana 5900
Frequency Counter	20 MHz capability 8 digit resolution ±2 count resolution	Dana 8015B
Distortion Analyzer	Fundamental frequencies to 10k Harmonics to 3 MHz 50 μV sensitivity	HP331A
Spectrum Analyzer	1 to 80 MHz range ±0.5 dB amplitude accuracy Noise >70 dB below reference	HP141T, HP8552B, and HP8553B
Calculator	IEEE 488-1975 compatible	HP9825

Table 2-4. Operation Verification

Step	Test	Tester and Setup	Program	Desired Results
1	Self Test	None.	Power ON	172B displays "SELF TEST"; then in <5s, "WAVETEK 172B".
2	Open Loop	Oscilloscope. Connect to 172B 50Ω OUT with a 50Ω load at the scope input. Set for 2V/div, horizontal 0.1 μs/div.	FREQ 10E6 AMPL DEF 0 AMPL 10 FUNC 0 MODE 0 OUTP 0 SYM 0 OFST 0 EXEC	1 cycle/div sine wave, 10V p-p.

Table 2-4. Operation Verification (Continued)

Step	Test	Tester and Setup	Program	Desired Results
3	Functional		FUNC 1 FREQ 5E6 EXEC	1 cycle/2 div triangle wave, 10V p-p.
4			FUNC 2 EXEC	1 cycle/2 div square wave, 10V p-p.
5			FUNC 4 OFST 2 EXEC	2 Vdc with no waveform.
6		Oscilloscope. Set horizontal to 2 μs/div.	FREQ 99.9E3 OFST 0 AMPL 5 SYM 2 FUNC 2 EXEC	+2.5V for 2 μs; −2.5V for 8 μs.
7			SYM 8 EXEC	+2.5V for 8 μs; −2.5V for 2 μs.
8	Sync Out	Oscilloscope. Connect to 172B SYNC OUT.		Pulse at same frequency and symmetry as 50Ω OUT signal.
		NOTE: Allow 1 hour warm-up before performing the following tests.		
9	Amplitude Accuracy	Voltmeter. Set to Vrms. Connect to 172B 50Ω OUT with no 50Ω load.	FREQ 999 AMPL DEF 1 AMPL 5.29 OUTP 1 SYM 5 FUNC 0 OFST 0 MODE 0 EXEC	5.283 to 5.316 Vrms.
10			AMPL 0.9 EXEC	0.897 to 0.903 Vrms.
11		Set voltmeter to dc.	FUNC 4 OFST 7.49 EXEC	7.46 to 7.52 Vdc.
12	Frequency Accuracy	Frequency Counter. Connect to 172B 50Ω OUT.	FREQ 12.9999E6 AMPL 1 OFST 0 FUNC 2 EXEC *Standard 172B:* MODE 0 EXEC *Option 002:* MODE 3 EXEC	Standard 172B: 12.6 to 13.4 MHz. Option 002: 12.9998 to 13.0000 MHz.
13			FREQ 1E6 EXEC	Standard 172B: 0.97 to 1.03 MHz. Option 002: 0.99999 to 1.00001 MHz.
14			FREQ 99.999E3 EXEC	Standard 172B: 96.9 to 103 kHz. Option 002: 99.998 to 100.000 kHz.

Table 2-4. Operation Verification (Continued)

Step	Test	Tester and Setup	Program	Desired Results
15	Harmonic Distortion	Distortion Analyzer. Connect to 172B 50Ω OUT. Set distortion meter to null, then to % distortion.	FREQ 3000 AMPL 5.29 FUNC 0 OUTP 1 EXEC	Total harmonic distortion under 0.5% (−46 dB).
16	Spurious	Spectrum Analyzer. Sweep from 0 to 100 MHz; video filter set to 10 kHz.	FREQ 10 AMPL 1 OUTP 0 EXEC	All discrete spurious −50 dBm or less.
17	Interface	Calculator. Connect to 172B GPIB connector. Set 172B rear panel address switch to 00001. Press 172B ADR key and verify GPIB address "1" on the display.	Calculator: 0: dim A$[100] 1: red 701,A$ 2: rem 7 3: clr 701 4: rds(701)→r1 5: stp	172B displays: "172B CLEARED R".
18			Calculator: 6: wrt 701,"....F10E3A 5D0P1I" 7: stp	172B displays: "FR 10E3 AM 5 OFS 0 RL".
19			172B: CMD RCL key	172B displays: "....F10E3A5D0P1IMJR RL" in last 22 characters.
20			Calculator: 8: wrt 701,"F1E9T1I" 9: stp	172B displays: "FR 10E3 AM 5 OFS 0 QRL".
21			Calculator: 10: red 701,A$ 11: dsp A$ 12: stp	Calculator displays: "E 1 F" setting error, frequency. 172B displays: "FR 10E3 AM 5 OFS 0 QRT".
22			Calculator: 13: wrt 701,"T2" 14: red 701,A$ 15: dsp A$ 16: stp	Calculator displays: "P E" (error poll). 172B displays: "TALK RESPONSE 2 SELECTED RT".
23			Calculator: 17: rds(701)→r2 18: dsp char(r2) 19: wrt 701,"'172B GPIB TEST COMPLETE'" 20: stp	172B displays: "172B GPIB TEST COMPLETE RL".

Table 2-5. Acceptance Test Record
(for reproduction)

Location _____

QA Inspector _____

Date _____

		Acceptable (✓)
A	Self Test and Functions (steps 1 through 8)	_____
B	Amplitude Accuracy	
	(9) value _____ Vrms	_____
	(10) value _____ Vrms	_____
	(11) value _____ Vdc	_____
C	Frequency Accuracy	
	(12) value _____ MHz	_____
	(13) value _____ MHz	_____
	(14) value _____ kHz	_____
D	Distortion	
	(15) value _____ %	_____
	(16)	_____
E	Interface-GPIB Operation (steps 17 through 23)	_____

SECTION 3
OPERATION

3.1 DATA ENTRY

Using the Model 172B is quite straight forward and is best understood by trial and error method while the microprocessor "converses" with you during operation, informing you what was programmed, what is possible to program and when an error is made. The example of data entry given in table 3-1 will give you the feel of using the 172B. Appendix B gives a summary of programming commands.

The details of power on, command structure and programming are given in paragraphs 3.2 and 3.3. Operation in each mode is discussed in paragraph 3.4. Front panel keyboard and readout are discussed in paragraph 3.5. Program functions peculiar to the GPIB are discussed in paragraph 3.6. These functions are in strict accordance to ground rules set forth in IEEE Standard 488-1975. The operation of the stored program facility is discussed in paragraph 3.7.

3.2 POWER

Power is turned on and off with a front panel pushbutton. When power is turned on, wait approximately 8 seconds before programming (for front panel option, wait until "WAVETEK MODEL 172B" is displayed). When the power is turned on, the generator automatically performs a self test routine. "SELF TEST" is displayed at this time. When testing is completed, "WAVETEK MODEL 172B" is displayed. At least two seconds must elapse between power OFF and power ON for proper reinitialization of logic. When the power comes on, the output is automatically disabled to allow loading of a program; line transients on the output are avoided. The generator must get an execute command to provide and output. (Refer to paragraph 3.3.8.)

Table 3-1. Example of Front Panel Data Entry

Instruction	Front Panel Entry (Press Keys)	Front Panel Display	Equivalent Program Entry
1. Power on.	OFF (becomes ON)	"SELF TEST", then within a few seconds, "WAVETEK MODEL 172B".	None
2. Check instrument address.	ADR	The state of the GPIB address switches will be displayed: GPIB = 1, 2, 3, or . . 30 (decimal address and ASCII listen and talk characters). (Refer to paragraph 2.2.4 to change addresses.)	G
3. Check initial conditions:			
Output and load	OUTP	OUTPUT OFF, 50 OHM LOAD OUT (2)	P
Amplitude	AMPL	AMPLITUDE 1 VOLT P-P	A
Offset	OFST	OFFSET 0 VOLTS	D
Frequency	FREQ	FREQUENCY 1 KILOHERTZ	F
Symmetry	SYM	SYMMETRY 50% (0)	S

Table 3-1. Example of Front Panel Data Entry (Continued)

Instruction	Front Panel Entry (Press Keys)	Front Panel Display	Equivalent Program Entry
Function	FUNC	FUNCTION IS SINE (0)	C
Mode	MODE	MODE IS CONTINUOUS (0)	B
4. Look at this signal by connecting the output to an oscilloscope with a 50Ω cable.	OUTP 1	LOAD 1	P1
5. Display a more descriptive readout of programming (for display only, not necessary in the programming sequence).	OUTP	OUTPUT ON, 50 OHM LOAD IN (1)	P
6. Execute the programming (it will now be available to the oscilloscope).	EXEC	FR 1E3 AM 1 OFS ϕ (this FR__AM__OFS__ format always comes on with EXEC; in this case, frequency of 1 kHz, amplitudeof 1V p-p and offset of 0V is output).	I
7. Look at the equivalent program character string.	CMD RCL	GPADFSCBP1IR (these are the equivalent program entries; see the last column in this table).	R
8. Reprogram the instrument:			
Ramp waveform	FUNC 1	FUNCTION 1	C1
	SYM 2	SYMMETRY	S2
5.1 kHz	FREQ 5 • 1 EXP 3	FREQUENCY 5.1E3	F5.1E3
14.9V p-p	AMPL 1 4 • 9	AMPLITUDE 14.9	A14.9
Offset −1.2 Vdc	OFST − 1 • 2	OFFSET −1.2	D−1.2
9. Initiate these new settings:	EXEC	WARNING: CLIPPING OR SYNTHESIZER ERROR (with the amplitude of 14.9V p-p and offset of −1.2 Vdc, peaks are 6.25V and −8.65V. Maximum allowable are ±7.5V; the negative peak will be clipped at −7.5V).	I
10. Change amplitude to 12.6V p-p.	AMPL 1 2 • 6	AMPLITUDE 12.6	A12.6
11. Initiate these settings.	EXEC	FR 5.1E3 AM 12.6 OFS −1.2 (no clipping occurs).	I

Refer to paragraph 3.5 for complete front panel data.

3.3 BASIC COMMAND STRUCTURE

The Model 172B is programmed by sending ASCII coded characters (refer to Appendix A) to the microprocessor via one of the two possible input ports (keyboard or GPIB) shown in figure 3-1. If input characters are present on more than one input port, they are read first from the GPIB and then from the keyboard. Thus, if the GPIB port is continuously supplied with characters, then no characters will ever be read from the keyboard.

Characters used to program the 172B are divided into classes:

1. Alphabetic characters — the characters A thru Z, except E.

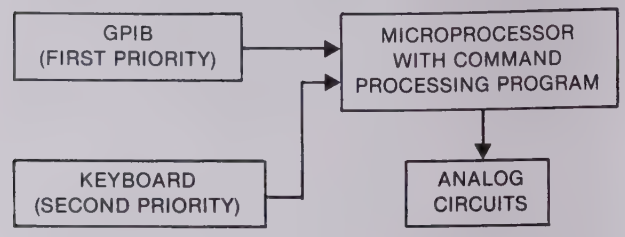


Figure 3-1. Instrument Processing Flow Diagram

2. Numeric characters — the characters 0 thru 9, E, −, decimal point (.).

3. Special character — Quote (').

4. Terminator character — initially the ASCII line feed character (LF). This can be changed by programming.

5. Nonprogramming characters — any character not in one of the above classes.

The alphabetic characters are used to select *actions* or *settings*. An action is a sequence of events which happens immediately when the character which selects it is read by the microprocessor. A setting is a numeric value which may be changed by programming. Table 3-2 lists the alphabetic characters and table 3-3 lists the numeric characters used.

To program an action, simply program the proper alphabetic character from either enabled port. The action will then take place, but only if the instrument is in the *enabled* state at the moment when that character is read by the microprocessor. (Refer to REN, paragraph 3.6.1.)

To examine the current value of a setting, simply program the proper alphabetic character from either input port. The current value will then be displayed on the front panel. This occurs whether or not the instrument is enabled. If the character programmed does not correspond to a legal setting in the instrument, nothing happens.

The numeric characters are used to program new setting values. To change a setting to a new value, first program the alphabetic character which selects the desired setting (F = frequency, etc.). The instrument must be enabled at this time, or it will not allow the new value to be entered. Next, program the new value using numeric characters; the instrument must be enabled for these as well. Any sequence of characters (called the argument of the setting) which gives the new value is acceptable. For example, all of the sequences in table 3-4 will cause the value 100 to be programmed.

The numbers to the left of the "E" are the mantissa; the digits to the right (only two are allowed) are the exponent. The result value is the mantissa times 10 to the exponent power.

Table 3-2. Alphabetic Characters Used in Model 172B*

ASCII Character	Keyboard Key	Action (A) or Setting (S)	Comments
A	AMPL	S	Amplitude
B	MODE	S	Mode
C	FUNC	S	Function
D	OFST	S	Offset and dc voltage
F	FREQ	S	Frequency
G	ADR	A	Display GPIB address
I	EXEC	A	Execute
J	TRIG	A	Trigger
M	STOR	S	Memorize program (refer to paragraph 3.7.1)
O	GET	A	GET mode
P	OUTP	S	50Ω load and output on/off
Q	SRQ	S	SRQ enable (refer to paragraph 3.6.5)
R	CMD RCL	A	Display last 37 programming input characters
S	SYM	S	Symmetry
T	TLK	S	Talk message specify (refer to paragraph 3.6.4)
U	LAST	A	Steps to previous numbered stored setting
V	AMPL DEF	S	Specify amplitude units (refer to paragraph 3.3.2.1)
W	NEXT	A	Steps to next higher numbered stored setting
X	TRM	S	Specify terminator character (refer to paragraph 3.6.6)
Y	RCL	S	Recall stored program (refer to paragraph 3.7.2)
Z	—	S	Same as Y**

*Characters not listed are not used.
**For compatibility with previous instruments.

Only one decimal point and one "E" (keyboard EXP) are allowed per number; additional ones are ignored. The sign toggle character may appear any number of times. It causes the sign of the mantissa (if "E" has not been programmed) or the exponent (if "E" has been programmed) to be reversed (if negative, then positive, and vice versa) each time it appears. Any number of nonprogramming characters may be interspersed with the numeric characters, as they have no effect. If an undesired value is entered, the CLR key can be used to erase it.

Table 3-3. Numeric Characters Used

ASCII Character	Keyboard Key	Function
0	0	Numeric digit
1	1	Numeric digit
2	2	Numeric digit
3	3	Numeric digit
4	4	Numeric digit
5	5	Numeric digit
6	6	Numeric digit
7	7	Numeric digit
8	8	Numeric digit
9	9	Numeric digit
.	.	Decimal point
–	+/–	Toggle sign
E	EXP	Indicates multiplication by 10 raised to a power

Several parameters require codes for specific selections; for example, the function codes of 0 thru 7 to select sine, triangle or square waves, etc. Refer to table 3-5 for parameter codes.

Since the number input format is so general, the microprocessor must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic, special or terminator character. When this is done, the new value is first tested to see if it is a legal value for the setting being changed. If it is not legal, an error message is displayed on the front panel, and the setting value is not changed. If it is legal, the new value is entered into the instrument's memory; however, it is not sent to the analog circuits. That can be done only by programming the "I" action (EXEC key on the front panel) or the Group Execute Trigger (GET).

When a new value is entered into the instrument memory, it is rounded to the number of significant digits specified by the setting being changed, as specified by table 3-6. Review table 3-1 for examples of command structure.

Table 3-4. Examples of Value Programming

ASCII	Keyboard	Standard Notation
100	100	100
0100	0100	100 (leading zeros are ignored)
1E2	1 EXP 2	1×10^2
.01E4	.01 EXP 4	$.01 \times 10^4$
.01E304	.01 EXP 304	$.01 \times 10^4$ (last two exponent digits only are used)
1000E-1	1000 EXP +/– 1	1000×10^{-1}
1E-2-	1 EXP +/– 2 +/–	1×10^2 (two minus signs cancel)
1E.2	1 EXP .2	1×10^2 (decimal points in exponent are ignored)

Table 3-5. Codes

Function (C) Codes	
Sine	0
Triangle	1
Square	2
DC	4
+ Pulse	6
– Pulse	7

Mode (B) Codes	
Continuous	0
Triggered	1
Gated	2
Synthesized (option)	3
Triggered Haverwave	4
Gated Haverwave	5
External Phase Lock	6

Output Load (P) Codes	
Load Out, Output On	0
Load In, Output On	1
Load Out, Output Off	2
Load In, Output Off	3

Symmetry (S) Codes	
50%	0,5 or 50
10% - 90%	1-9 or 10-90

Ampl (V) Codes	
V p-p into 50Ω	0
Vrms	1
dBm	2

Talk (T) Codes	
Status	0
Error Status	1
Service Request Status	2
Value of Setting	4

GET (O) Codes	
Select Previous Numbered Stored Setting and Trigger	-1
Trigger on GET	0
Select Next Numbered Stored Setting and Trigger	1

Table 3-6. Round Offs

Letter	Setting Name	Number of Digits
A	Amplitude	3 if setting is less than 10 4 if setting is greater than or equal to 10 *For example:* *1.5 (not rounded, has only 2 digits)* *1.853 (1.85)* *96.56E-1 (9.66)* *14.997 (15.00), illegal ampl*
O	Offset	3
F	Frequency	If synthesizer is installed: 5 if setting is less than 10 MHz 6 if setting is greater than or equal to 10 MHz If synthesizer option is not installed: 3 if setting is less than 10 MHz 4 if setting is greater than or equal to 10 MHz
S	Symmetry	1
All other settings		Nearest integer

3.3.1 Frequency

"F" followed by its argument denotes frequency in hertz. The argument value may be between 1.000×10^{-4} and 1.29999×10^{7}, fixed or floating. Refer to table 3-6 for round offs. In addition, the special argument value of zero is permitted. When this is programmed, the frequency magnitude is set to zero, but the range is left at its previously programmed value. This facility allows calibration and wide ranging analog voltage controlled frequency sweeps.

3.3.2 Amplitude

3.3.2.1 Amplitude Definition

"V" followed by its argument selects the amplitude programming mode. The argument may be 0, 1 or 2. Round off is to one digit.

0 Selects volts peak-to-peak into 50Ω

1 Selects Vrms

2 Selects dBm

3.3.2.2 All Waveforms

"A" followed by its argument denotes amplitude (in volts peak-to-peak into 50Ω, in Vrms or in dBm, depending on the amplitude mode code (refer to paragraph 3.3.2.1). The argument value may be between 1.00×10^{-3} and 1.499×10^{1} (1 mVrms to 5.3 Vrms, −56 to 27.4 dBm), fixed or floating. Round off is to 3 digits to 10V p-p and to 4 digits from 10 to 15V p-p. A minus sign in the mantissa will invert the waveform.

NOTE

When offset is used, three digit resolution of offset or amplitude may be reduced in some cases. (Refer to paragraph 3.3.3.)

3.3.2.3 Pulses

The positive and negative pulses are special cases of the offset square wave. The pulses are square waves that the microprocessor automatically offsets, so that the negative peak in + pulse mode and the positive peak in the − pulse mode are always at zero volts, regardless of the amplitude programmed. With this in mind, the rules and notation used in paragraphs 3.3.2.2 and 3.3.3 are applicable to the pulses.

3.3.3 Offset and DC Voltage

"D" followed by its argument denotes offset (or, with no waveform, dc voltage) value in volts. (Offset is in volts regardless of amplitude mode.) The argument may be between −7.49 and 7.49 and may be a fixed or floating point. Round off is to 3 digits. The combined waveform and offset cannot exceed ±7.5V peak. As offset is increased, it is usually necessary to decrease the waveform peak-to-peak amplitude to stay within the peak limit; otherwise, waveform clipping will result.

The amplitude and offset are not completely independent of one another, because they share a common output amplifier and attenuator (see figure 3-2). In certain cases it may be necessary to decrease the number of digits of resolution of amplitude or offset in order to prevent clipping in the output amplifier or to make the programmed value of offset (or amplitude) appear at the output despite an unfavorable attenuator setting necessitated by a larger value of amplitude (or offset).

The sum of amplitude and offset control the output amplifier and attenuator. The output amplifier is limited

to ±7.5 volts peak and a 3 digit input (X.XX), and the attenuator can operate at only one value, $\times 10^{0}$, $\times 10^{-1}$, $\times 10^{-2}$ or $\times 10^{-3}$.

If the *absolute peak value* at the amplifier is ever 7.50 or greater, logic decreases the amplifier input (amplitude + offset) by a factor of 10 and, to maintain the same value, decreases attenuation by a factor of 10 also.

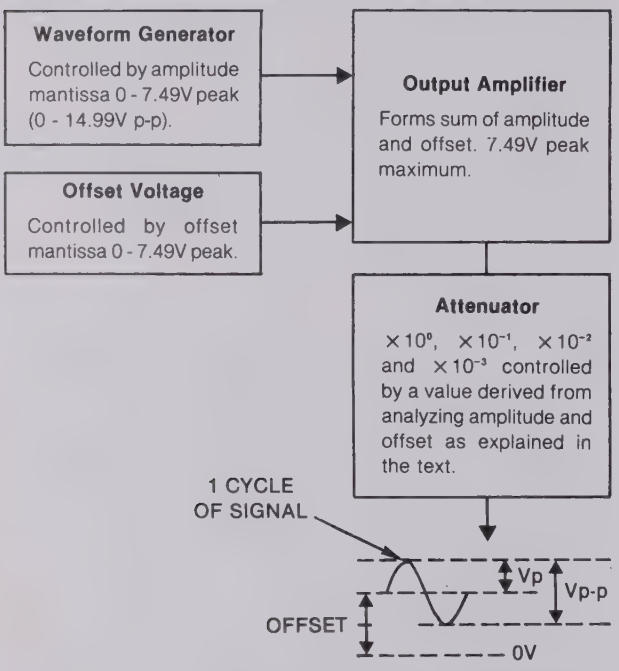

Waveform Generator
Controlled by amplitude mantissa 0 - 7.49V peak (0 - 14.99V p-p).
Offset Voltage
Controlled by offset mantissa 0 - 7.49V peak.
Output Amplifier
Forms sum of amplitude and offset. 7.49V peak maximum.
Attenuator
×10⁰, ×10⁻¹, ×10⁻² and ×10⁻³ controlled by a value derived from analyzing amplitude and offset as explained in the text.
1 CYCLE OF SIGNAL
Vp
Vp-p
OFFSET
0V

Figure 3-2. Hardware Diagram of Amplitude and Offset Generation

To determine if there is clipping or loss of resolution, perform the following calculation (amplitude in volts peak-to-peak).

1. Add the absolute value of the desired offset value to ½ the absolute value of the desired amplitude. If the sum exceeds 7.49, clipping will occur. If not, go on to step 2 to determine if loss of resolution will occur.

2. Write the larger of the absolute amplitude or absolute offset in the form $N.NN \times 10^{x}$, where N.NN is between 1.00 and 9.99.

3. Take the sum of amplitude and offset computed in step 1 and write it in the form $MM.MM \times 10^{x}$, where x is the exponent computed in step 2. If MM.MM is greater than 7.49, then one digit of resolution must be lost from both amplitude and offset in order to prevent the output amplifier from clipping.

4. Perform this step, if step 3 did not result in a loss of resolution. Write the amplitude or offset, whichever is smaller in absolute value, in the form $YY.YYZZZ \times 10^{x}$, where x is the exponent computed in step 2. If any of the digits in ZZZ are nonzero, then resolution is lost, because only YY.YY can be used to program the waveform generator circuits.

Example A

Ampl = −3.43
Offset = 4.25

Step 1 $4.25 + 1.72 = 5.97$. *There is no clipping.*

Step 2 *Absolute offset is larger.*
$4.25 = 4.25 \times 10^{0}$. *Therefore,* $x = 0$.

Step 3 $5.97 = 5.97 \times 10^{0}$. *Therefore, there is no loss of resolution in either parameter.*

Step 4 *Absolute amplitude is smaller.*
$-3.43 = 3.43000 \times 10^{0}$. *Therefore, there is no loss of resolution anywhere.*

Example B

Ampl = .0964
Offset = .720

Step 1 $.720 + .0482 = .7682$. *There is no clipping.*

Step 2 $.720 = 7.20 \times 10^{-1}$. $x = -1$.

Step 3 $.7682 = 7.682 \times 10^{-1}$. *Since 7.682 exceeds 7.49, there will be a loss of one digit of resolution in both amplitude and offset. This means that the offset will be .720 and the amplitude will be .096 (not .0964).*

Step 4 *Not required.*

Example C

Ampl = 2.58
Offset = .123

Step 1 $.123 + 1.29 = 1.413$. *There is no clipping.*

Step 2 *Absolute amplitude is larger.*
$2.58 = 2.58 \times 10^{0}$. *Therefore,* $x = 0$.

Step 3 $1.413 = 1.413 \times 10^{0}$. *No loss of resolution so far.*

Step 4 *Absolute offset is smaller.*
$.123 = 0.12300 \times 10^{0}$. $YY.YY = 00.12$, $ZZZ = 300$. *Therefore, one digit is lost in the offset, which will be .120, not .123.*

3.3.4 Function

"C" followed by its argument denotes waveform selection. The argument may be one of the following. Round off is to nearest integer.

0 Selects sine wave

1 Selects triangle wave

2 Selects square wave

4 Selects dc voltage

6 + pulse

7 − pulse

3.3.5 Mode

"B" followed by its argument selects instrument mode. The argument may be 0 to 6. Round off is to one digit. The following modes are illustrated in figure 3-3.

0 Selects continuous. The generator runs continuously with parameters as programmed.

1 Selects triggered. The generator is quiescent until a negative going TTL pulse is fed to the TRIG IN BNC, the TRIG key is pressed, a "J" is programmed or a GET is programmed, which causes one cycle of the selected waveform to be generated.

2 Selects gated. The generator is quiescent until a negative going TTL pulse is fed to the TRIG IN BNC, which causes the generator to run for the duration of the pulse.

3 Selects synthesized (an option). The generator is phase locked to a frequency synthesizer for 5½ digit frequency resolution. (Refer to paragraph 1.2 for signal accuracy and purity.)

4 Selects triggered haverwave. As for triggered except the quiescent level is at the negative peak voltage (can be offset or inverted for desired level).

5 Selects gated haverwave. As for triggered haverwave except the generator runs continuously for the duration of the TTL level pulse fed to the TRIG IN BNC.

6 Selects external phase lock. When programmed within 2% of the TTL-level 10 Hz to 13 MHz signal present at the ϕ LOCK IN BNC, the generator phase locks to that reference signal.

Figure 3-3 shows the waveforms and their phase relationship relative to the sync output and two controlling input signals: trigger and phase reference. The waveforms are sine, triangle and square plus their inverted forms. In the continuous mode, a trigger input has no effect, and in trigger and gated modes, phase reference input has no effect.

In triggered and gated modes, notice that square waveforms do not change state immediately upon being triggered. Trigger duration has no effect on triggered output, but does on gated output. The cycle count on the gated sine wave shows that when the gate signal ends in the shaded area; that is, between the positive peak of cycle 2 and positive peak of cycle 3, cycle 3 will be completed. In the haverwave modes, waveforms start at a peak value; all other waveforms are normally symmetrical about signal ground. Notice the symmetry control effects shown in one series of waveforms. Symmetry may be set at any multiple of 10% from 10 to 90%. Fifty percent is normal symmetry.

3.3.6 Load and Output

"P" followed by its argument selects the output and internal 50Ω load status. The argument may be 0 to 3. Round off is one digit.

0 Disconnects the internal load and connects the generator directly to the outside circuit.

1 Connects the internal load and connects the generator to the outside circuit.

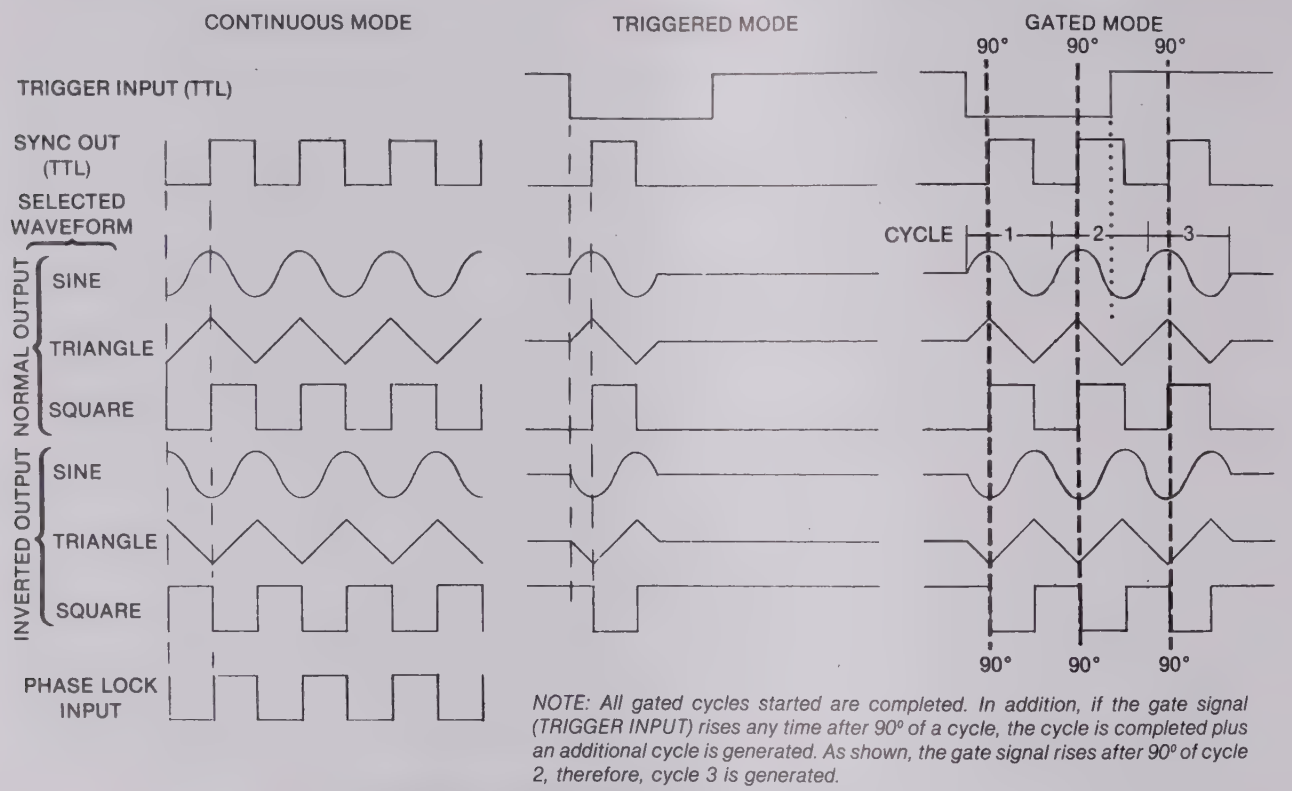
2 Disconnects generator output and disconnects internal load.

3 Disconnects generator output and connects internal load to the outside circuit.

3.3.7 Symmetry

"S" followed by its argument controls the percent of on, or active, time of the total time for the selected signal. Symmetry operates on frequencies up to 999,990 Hz. Round off is to one digit.

The argument may be 0 to 9 or 10 to 90. Round off one digit. The effect of symmetry control is illustrated in figure 3-1.



NOTE: All gated cycles started are completed. In addition, if the gate signal (TRIGGER INPUT) rises any time after 90° of a cycle, the cycle is completed plus an additional cycle is generated. As shown, the gate signal rises after 90° of cycle 2, therefore, cycle 3 is generated.

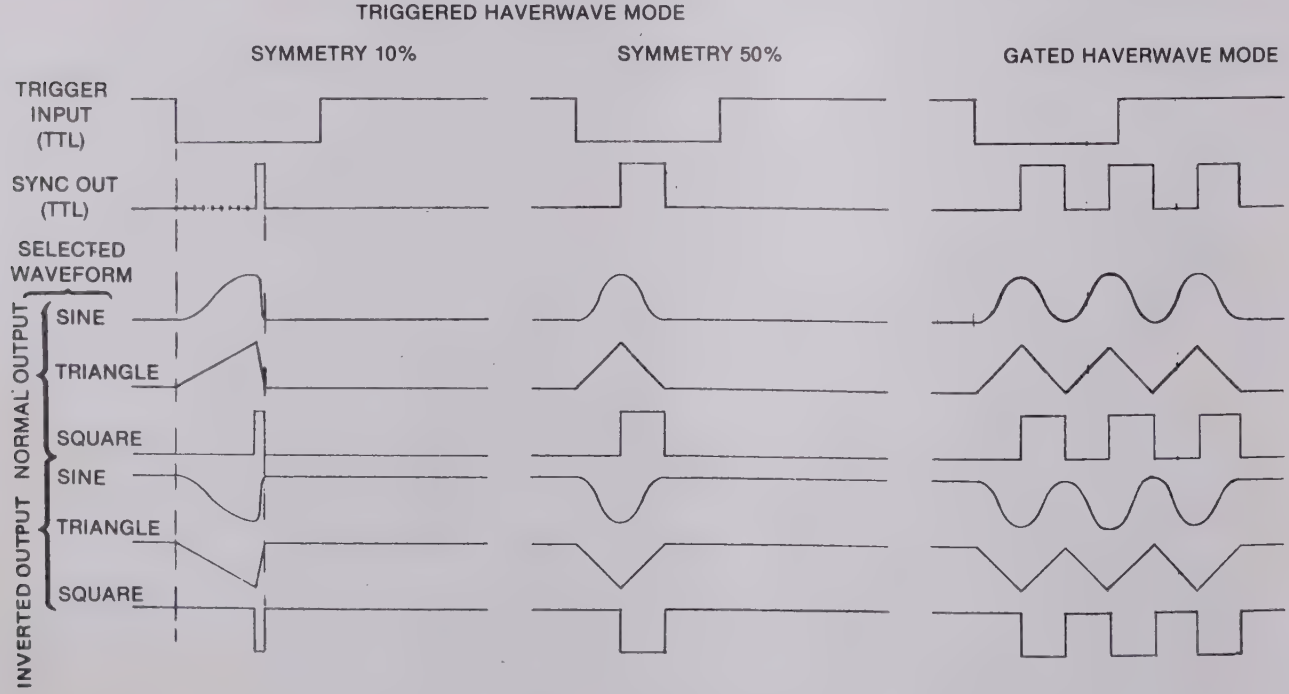


Figure 3-3. Waveforms for Each Mode

0, 5 or 50 selects 50%

1 or 10 selects 10%

2 or 20 selects 20%

9 or 90 selects 90%

3.3.8 Executing the Program

"I" without an argument transfers the programmed values to the waveform generator circuits; that is, executes the program. No waveform changes can be made except with this command. This action also checks the following groups of parameters for consistency.

1. Amplitude and offset — an error is signalled if their combined values are so high that clipping occurs in the output amplifier.

2. Frequency and mode — an error is signalled if the mode is synthesized and the frequency is below 10 Hz.

NOTE

Individually valid programmed setting values are sent to the waveform generator circuits whether or not a consistency error is found.

Execution of a program can also be commanded with the GPIB Group Execute Trigger (GET) command. In this case no error checking is done.

3.3.9 GPIB Address

"G" without an argument causes the address to be displayed. The address (0 to 30) is set by a set of switches on the rear panel.

3.3.10 Trigger

"J" without an argument causes a trigger pulse to be sent to the analog circuits when in triggered or triggered haverwave mode. This has the same effect as applying a trigger pulse to the TRIG BNC, pressing the keyboard TRIG or programming a GET.

3.3.11 Command Recall

"R" without an argument will display the last 37 characters sent to the instrument. These characters are not returned to the controller over the GPIB. The display uses a 64 character subset of the full 128 character ASCII code: character codes 20_{16} thru $5F_{16}$. The other characters are displayed as the first set of 64; they are mapped into the first set by their six least significant digits. This function is used for troubleshooting. This character has additional stored program functions. (Refer to paragraph 3.7.2.)

3.3.12 Errors

When a nonlegitimate argument is programmed, an error message is generated. If an error occurs in a programmed setting, the previous value is retained. If the error was caused by programming from the front panel, an error display will appear on the front panel display. If the error was caused via the GPIB, a service request will be made if service request is enabled (refer to paragraph 3.6.5).

3.4 OPERATING MODES

3.4.1 Initial Conditions

At power on, the instrument is set as follows: 1 kHz, 1V p-p, continuous, symmetrical sine wave with the output off and the internal 50Ω load not in the circuit.

3.4.2 Operating as a Basic Waveform Generator

When operating as a basic waveform generator, the generator runs continuously with parameters as programmed.

1. Make rear panel 50Ω OUT and SYNC OUT connections for signal and sync, as required.

2. Refer to paragraph 3.6 if programming remotely.

3. The output must be programmed on (P0 or P1). (Refer to paragraph 3.3.6.) The mode must be continuous (B0). (Refer to paragraph 3.3.5.)

4. Program the desired waveform, symmetry, frequency, amplitude and offset. (Refer to paragraphs 3.3.1 through 3.3.4 and 3.3.7.)

5. Execute the program. (Refer to paragraph 3.3.8.)

3.4.3 Operating as a Triggered or Gated Generator

See figure 3-3 for mode and waveform illustrations.

Triggered — The generator is quiescent until a negative going TTL pulse is fed to the TRIG IN

Triggered (Cont)	BNC, the TRIG key is pressed or a "J" or GET is programmed, which causes one cycle of the selected waveform to be output.
Gated	As for triggered, except the generator runs continuously for the duration of the TTL level pulse fed to the TRIG IN BNC.
Triggered Haverwave	As for triggered except the quiescent level is at the negative peak voltage (can be offset or inverted for desired level).
Gated Haverwave	As for triggered haverwave except the generator runs continuously for the duration of the TTL level pulse fed to the TRIG IN BNC.

1. Make rear panel 50Ω OUT and SYNC OUT connections for signal and sync, as required.
2. Refer to paragraph 3.6 if programming remotely.
3. The output must be programmed on (P0 or P1). (Refer to paragraph 3.3.6.) The mode must be triggered (B1), triggered haverwave (B4), gated (B2) or gated haverwave (B5). (Refer to paragraph 3.3.5.)
4. Program the desired waveform, symmetry, frequency, amplitude and offset. (Refer to paragraphs 3.3.1 through 3.3.4 and 3.3.7.)
5. Execute the program. (Refer to paragraph 3.3.8.) The generator has no output until a trigger signal is applied.
6. If triggering with a TTL signal at the TRIG IN BNC or gating, apply a TTL low at the TRIG IN BNC for one cycle of waveform (triggered or triggered haverwave mode) or a burst of waveform for the duration of the TTL low (gated or gated haversine mode). If triggering at the front panel, press TRIG. If triggering on the bus, program a "J" or a GET.

3.4.4 Operating as a Voltage Controlled or Frequency Modulated Generator

VCG operation is the same as the basic waveform operation (refer to paragraph 3.4.2) plus the connection of a VCG voltage source to the VCG (FM) IN connector. Input impedance is 5 kΩ. Input is disabled when mode is synthesized or external phase lock.

The VCG input, either dc or ac, can be used to externally control the frequency of the 50Ω OUT signal. A positive voltage applied to the VCG IN connector will increase the generator frequency, and a negative voltage will decrease the frequency within the range of operation.

Figure 3-4 illustrates the voltage required to change the programmed frequency to a desired output frequency. For example, if 500 Hz is programmed frequency, a 2.5 volt VCG input will change the frequency to 1 kHz. Frequency can only be changed within a range and is limited in each range according to figure 3-5. Range is defined as an exponent of the ×10 multiplier (see figure 3-5).

For wide range sweeping with a zero to a positive sweep voltage, use the special zero-frequency capability. Set frequency mantissa to zero (F0I) to set a frequency under the lower defined limits of figure 3-5. The range remains as the last frequency range set.

3.4.5 Operating as a Frequency Synthesizer (an Option)

The generator with synthesizer option is phase locked to a frequency synthesizer for 5½ digit frequency resolution. (Refer to paragraph 1.2 for signal accuracy and purity.)

1. Make 50Ω OUT, SYNC OUT, REF IN and REF OUT connections for signal and sync, as required.

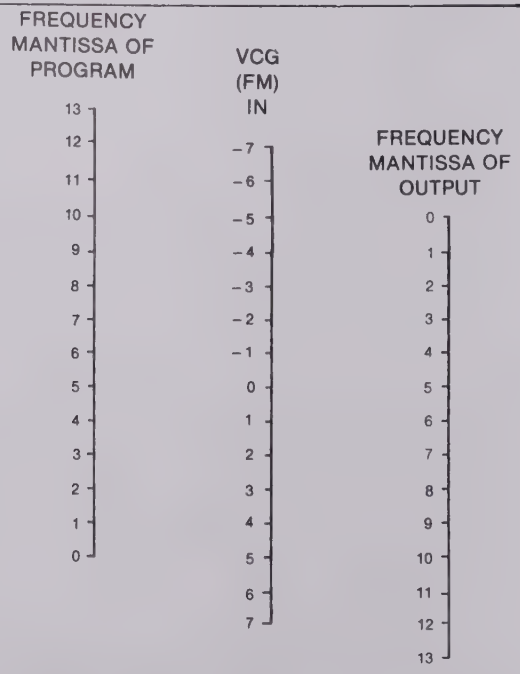
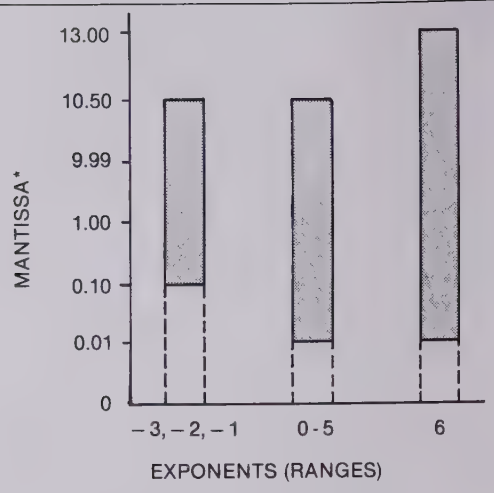


Figure 3-4. VCG (FM) Nomograph



*When program is stated with one digit to the left of the decimal (or two digits to the left of the decimal for values ≥ 10 in the 10^6 range).

Figure 3-5. VCG Range Limits

2. If an external 10 MHz reference is to be used, apply the signal to REF IN. (This signal is then available at REF OUT.) To use an external reference signal, apply a sine or square wave within ±3 ppm of 10.0 MHz, 1 to 10 Vrms and 50 ± 8% duty cycle to the REF IN BNC.

3. Refer to paragraph 3.6 if programming remotely.

4. The output must be programmed on (P0 or P1). (Refer to paragraph 3.3.6.) The mode must be synthesized (B3). (Refer to paragraph 3.3.5.)

5. Program the desired waveform, symmetry, frequency, amplitude and offset. (Refer to paragraphs 3.3.1 through 3.3.4 and 3.3.7.)

6. Execute the program. (Refer to paragraph 3.3.8.)

3.4.6 Operating as a DC Voltage Source

DC voltage output amplitude is programmed as offset. Attenuation can be programmed directly in this mode.

1. Refer to paragraph 3.6 if programming remotely.

2. The output must be programmed on (P0 or P1). (Refer to paragraph 3.3.6.) The function must be DC (C4). (Refer to paragraph 3.3.4.)

3. Program offset for the desired dc amplitude. (Refer to paragraph 3.3.3.)

4. Execute the program. (Refer to paragraph 3.3.8.)

3.4.7 Operating as a Phase Lock Generator

When programmed within 2% of the TTL level 10 Hz to 13 MHz signal present at the ϕ LOCK IN BNC, the generator phase locks to that reference signal.

1. Refer to paragraph 3.6 if programming remotely.

2. The output must be programmed on (P0 or P1). (Refer to paragraph 3.3.6.) The mode must be external phase lock (B6). (Refer to paragraph 3.3.5.) Program the frequency to within 2% of the external reference frequency.

3. Program the desired waveform, symmetry, amplitude and offset. (Refer to paragraphs 3.3.1 through 3.3.4 and 3.3.7.)

4. Apply the 10 Hz to 13 MHz reference signal to the ϕ LOCK IN BNC.

5. Execute the program. (Refer to paragraph 3.3.8.)

3.5 FRONT PANEL OPTION

3.5.1 Keyboard and Display

Keyboard controls are listed in tables 3-2 and 3-3. Readout for the key functions are listed in table 3-7. Readout is literal and in two slightly different modes; for example, for frequency, amplitude and offset. When FREQ, AMPL or OFST keys are pressed, as for an inquiry as to status, the words MICROHERTZ, MILLIVOLTS, etc., are used, whereas when the operator starts keying in the parameter argument, no unit of measure is displayed. Coded parameters, such as symmetry, function, mode and output, show their programmed argument in parentheses.

3.5.2 Display

The single quote character (') is used to cause a string of characters to be displayed on the front panel self-scan display. This is accomplished by first programming a single quote, then the characters to be displayed, followed either by another single quote or by the terminator character. When the second quote or the terminator is programmed, the first 37 characters programmed after the first quote are displayed on the front panel. If fewer than 37 characters are programmed, then blanks are added to fill the display.

Examples (∧ indicates a blank character):

Table 3-7. Key and Readout

Key	Readout (lower case words added for understanding only)
ADR	GPIB = (Decimal Address, ASCII listen character and ASCII talk character)
AMPL DEF	AMPLITUDE IN VOLTS PEAK-TO-PEAK (0) or AMPLITUDE IN VRMS (1) or AMPLITUDE IN DBM (2)
CMD RCL	Lists last 37 characters programmed (refer to tables 3-2 and 3-3)
OUTP	OUTPUT ON, 50 OHM LOAD OUT (0) or OUTPUT ON, 50 OHM LOAD IN (1) or OUTPUT OFF, 50 OHM LOAD OUT (2) or OUTPUT OFF, 50 OHM LOAD IN (3)
FREQ	FREQUENCY _____ MICROHERTZ or _____ MILLIHERTZ or _____ HERTZ or _____ KILOHERTZ or _____ MEGAHERTZ
AMPL	AMPLITUDE _____ MILLIVOLTS or _____ VOLTS
OFST	OFFSET _____ MILLIVOLTS or _____ VOLTS
SYM	_____ % SYMMETRY (0, 1, 2, - - - or 9)
FUNC	FUNCTION IS SINE (0) or TRIANGLE (1) or SQUARE (2) or DC (4) or + PULSE (6) or – PULSE (7)
MODE	MODE IS CONTINUOUS (0) or TRIGGERED (1) or GATED (2) or SYNTHESIZED (3) or TRIGGERED HAVERWAVE (4) or GATED HAVERWAVE (5) or EXTERNAL PHASE LOCK (6)
EXEC	FR (frequency) AM (amplitude) OFS (offset)
TRIG	172 TRIGGERED
CLR ENTY	Clears any unexecuted setting of the last parameter entered
SRQ	SRQ ENABLED or SRQ NOT ENABLED
TLK	TALK RESPONSE (0, 1, 2 or 4) selected
TRM	TERMINATOR IS: (ASCII character) (decimal value)
+/–	"–" or blank (implies "+")
GET	PREVIOUS STORED SETTING ON GET (–1) or EXECUTE AND TRIGGER ON GET (0) or NEXT STORED SETTING ON GET (1)
STOR	SETTING ____ STORED or SETTING ____ DELETED (1 through 240)
RCL, NEXT, LAST	SETTING ____ RECALLED

NOTE: The three right-most characters of the display will show the status of the GPIB interface: a "Q" after an error has occurred, an "R" when in remote control, and a "T" for Talk or an "L" for Listen.

Three Programmed Inputs

1. 'THIS^IS^A^29^CHARACTER STRING'
2. 'THIS^STRING^IS^TOO^LONG^TO^DISPLAY^ENTIRELY'
3. '' (no character in string)

The Resulting Displays

1. THIS^IS^A^29^CHARACTER^STRING^^^^^^^^
2. THIS^STRING^IS^TOO^LONG^TO^DISPLAY^EN
3. (blank display)

3.6 GPIB INTERFACE

The GPIB interface is an implementation of IEEE Standard 488-1975. It supports the following interface functions: Source Handshake (SH1), Acceptor Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL1), Device Clear (DC1) and Device Trigger (DT1). Devices connected to the GPIB can have one or more of the three capabilities: talk, listen and control. The talk capability allows a device to send data (such as voltmeter or counter readings) out over the bus. The listen capability allows a device to receive data (such as device programming information or a printer receiving data to be printed) from the bus. The control capability allows a device to control the flow of data over the bus. Although there may be more than one device connected to the GPIB with control capability, only one device at a time may exercise that capability on the bus. One device's control capability must be active at all times; this device is called the controller.

Programming examples are given in Appendix C.

Table 3-8. GPIB Lines and Commands

Bus Lines	
DIO1 - DIO8	Data In/Out Lines
ATN	Attention
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
REN	Remote Enable
SRQ	Service Request
IFC	Interface Clear
GPIB Commands	
Listen Address	
Talk Address	
Secondary Address	
Universal Commands	
DCL	Device Clear
SPE	Serial Poll Enable
SPD	Serial Poll Disable
Addressed Commands	
GTL	Go To Local
SDC	Selective Device Clear
GET	Group Execute Trigger

3.6.1 Bus Lines Defined

The GPIB consists of 16 signal lines, as shown in table 3-9. Their functions are:

DIO1-DIO8 These eight lines (Data In/Out) are used to send commands and data encoded as 8 bit binary numbers (bytes).

ATN This line (Attention) is operated only by the controller. It specifies whether the information on lines DIO1-DIO8 is data (false) or a command (true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages; additionally, every device connected to the bus is required to receive and process every command sent by the controller.

DAV, NRFD, NDAC These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle must occur. This handshake is designed to hold up the bus until the slowest device has accepted the information.

EOI When ATN is false, this line (End Or Identify) indicates that the data on lines DIO1-DIO8 is (true) or is not (false) the last byte of a data message. When the 172B receives a data byte with EOI true, it automatically supplies a terminator character (refer to paragraph 3.6.6) following the data byte. When the 172B transmits the last byte of a message (which is always a terminator character), it also sets EOI true.

REN This line (Remote Enable) is used to control whether devices on the GPIB are in local or remote mode. In local mode, devices respond to front panel commands and do not respond to GPIB originated commands. In remote mode, the situation is reversed: GPIB originated commands are obeyed, while front panel commands are ignored. A device enters the remote state whenever it receives its listen address (refer to paragraph 3.6.2.1) at the same time as REN is in the remote state. The device then stays in the remote mode until either the REN line is put in the local state or the device receives a Go-To-Local (GTL) command or the LOCAL front panel key is pressed while the interface is not in the local lockout state (refer to paragraph 3.6.2.4d).

SRQ This line (Service Request) is used by the devices on the bus to signal the controller that they need attention. (Refer to paragraph 3.6.5 for 172B Service Request Enable.) Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signalling. The Serial Poll capability is usually employed to accomplish this.

IFC This line (Interface Clear) is used by the controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.6.2 GPIB Commands

Commands are sent over lines DIO1 - DIO8 with ATN true. They are divided into five classes.

3.6.2.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1 - DIO8. There are 31 different available addresses (hexadecimal codes 20 thru 3E, ASCII codes "SP" thru ">"). A 32nd address, called unlisten (hexadecimal 3F, ASCII "?"), is used to command all devices not to read data bytes. The 172B listen address is selected by the rear panel DIP switch, which specifies the lower 5 bits of the address. (Refer to table 2-2.)

3.6.2.2 Talk Addresses

Talk addresses are used to command a device to transmit data over lines DIO1 - DIO8 whenever ATN is false. There are 31 different available addresses (hexadecimal codes 40 thru 5E, ASCII codes "@" thru "↑"). A 32nd address, called untalk (hexadecimal 5F, ASCII "←") is used to command all devices to cease talking. The lower 5 bits of the 172B talk address are selected by the same rear panel DIP switch used to select the listen address. Thus, if the 172B listen address is hexadecimal 21 (ASCII "!"), the talk address is hexadecimal 41 (ASCII "A").

3.6.2.3 Secondary Addresses

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the 172B.

3.6.2.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the 172B are:

1. Device Clear (DCL) — resets the following settings to the power on state.

AMPLITUDE	1 VOLT
OFFSET	0 VOLTS
FREQUENCY	1 kHz
MODE	CONTINUOUS
FUNCTION	SINE
LOAD	OUTPUT OFF, LOAD OUT
SYMMETRY	50%

This information is also set into the waveform generating circuitry.

2. Serial Poll Enable (SPE) — causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line (in particular, the status byte will be an "E", if service is being requested, zero, if not). When the status byte is read, it is reset to zero, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the 172B talk message number 2. When this message is read, the status byte is reset to 0 and SRQ released as for the serial poll.

3. Serial Poll Disable (SPD) — removes the instrument from the serial poll mode activated by the SPE command.

4. Local Lockout (LLO) — causes the GPIB interface to enter a state where the front panel LOCAL key is inoperative. Once in this state, the only way to take the interface out of it is to put the REN line in the local state (refer to paragraph 3.6.1). Local lockout must be sent to the 172B to totally disable front panel modification of the state of the instrument.

3.6.2.5 Addressed Commands

Address commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a listener. Addressed commands performed by the 172B are:

1. Go To Local (GTL) — commands the 172B to go to the local mode (refer to paragraph 3.6.1 for explanation of REN line).

2. Selective Device Clear (SDC) — causes the same action as for Device Clear (DCL) command (refer to paragraph 3.6.2.4).

3. Group Execute Trigger (GET) — causes the same actions as specified by the GET mode ("O") argument (refer to paragraph 3.6.7). If the 172B's microprocessor is idle (i.e., not processing a previously sent programming string), a GET command will be completed within 2 ms of receipt. Otherwise, it will not be done until current programming is processed.

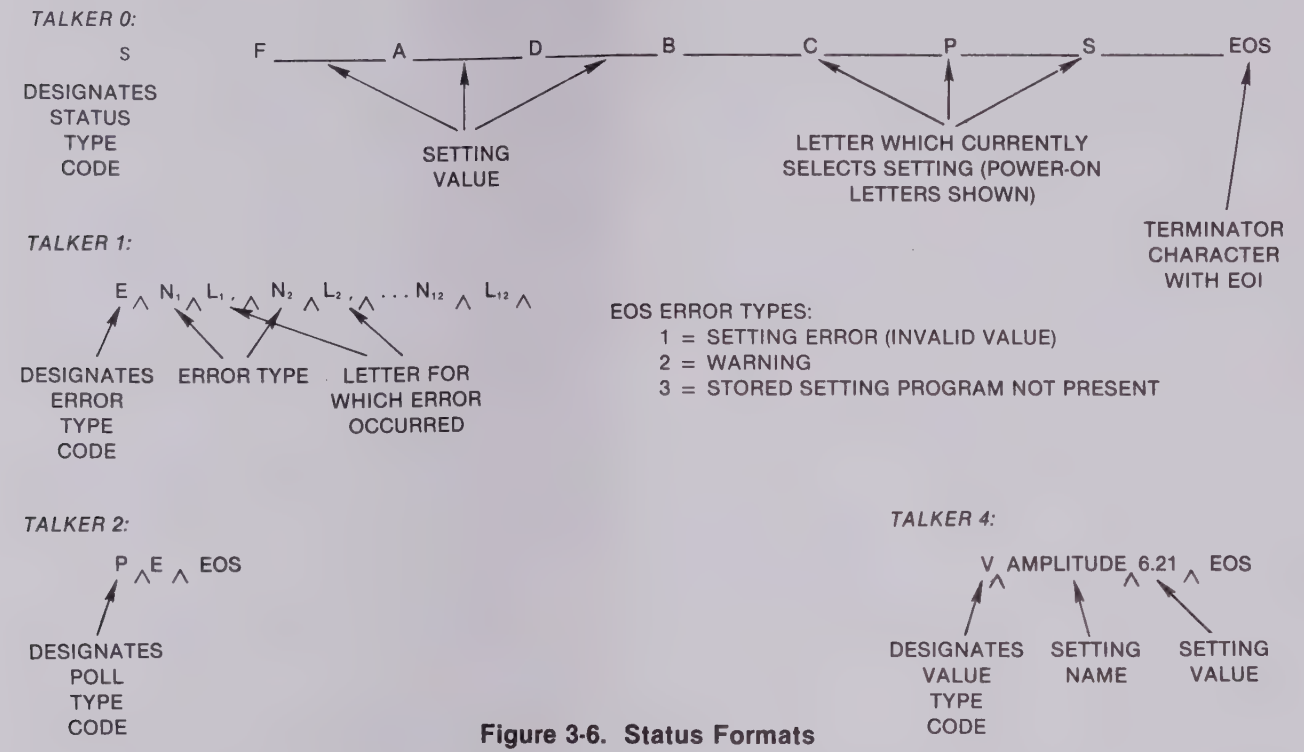

TALKER 0:
S
DESIGNATES STATUS TYPE CODE
F A D B C P S EOS
SETTING VALUE
LETTER WHICH CURRENTLY SELECTS SETTING (POWER-ON LETTERS SHOWN)
TERMINATOR CHARACTER WITH EOI
TALKER 1:
E N1 L1 , N2 L2 , . . . N12 L12
DESIGNATES ERROR TYPE CODE
ERROR TYPE
LETTER FOR WHICH ERROR OCCURRED
EOS ERROR TYPES:
1 = SETTING ERROR (INVALID VALUE)
2 = WARNING
3 = STORED SETTING PROGRAM NOT PRESENT
TALKER 2:
P E EOS
DESIGNATES POLL TYPE CODE
TALKER 4:
V AMPLITUDE 6.21 EOS
DESIGNATES VALUE TYPE CODE
SETTING NAME
SETTING VALUE

Figure 3-6. Status Formats

3.6.3 GPIB Data Transfers

The 172B will both accept programming characters and transmit status information over the bus. To program the instrument, first send the listen address (with ATN on), followed by the programming data (in ASCII, with ATN off). The instrument microprocessor accepts the data as fast as possible, until either 64 characters are received or there is a pause during the transfer of data. At that time, the entire string of received characters is scanned by the microprocessor, which carries out the programming instructions contained in it. While this is happening, the instrument can accept an additional 64 characters of data over the bus; if more are sent, the bus will hang until the microprocessor completes a scan and accepts the next 64 character string. Whenever the microprocessor finishes scanning a string, it puts a display on the front panel which reflects the state of input processing at that point. If the EOI line is asserted while sending a character to the 172B, the currently programmed terminator character will be put into the input string following the character with the EOI.

To read a message from the 172B, first send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Message Select (T) setting. The last character of this message will be the currently programmed terminator character with the EOI line asserted.

3.6.4 Talker

"T" followed by its argument sets the particular type of status message sent by the 172B when asked to talk on the GPIB (see Appendix C, example 2). The argument may be 0 thru 4, except 3. Round off is to one digit. The argument codes are:

0 Status message will give currently programmed waveform setting values. These will be the same as the values controlling the analog circuits if no new values were programmed since the last execute action. If this message is sent back to the 172B as programming input at a later time, it will restore the frequency, amplitude, offset, mode, function, output and symmetry settings to the values they had when the message was read from the 172B. (See figure 3-6.)

1 Status message will give a list of the first 12 errors since the last time this message was read from the instrument. After this message is read, the list of errors is cleared to blanks, so that a subsequent read will get only "E" until another error happens.

2 Status message contains the status byte which describes why the instrument is requesting service on the GPIB. It is the same byte which is read by a serial poll. Reading this message also turns off the service request if it was on. In the standard instrument, the only value defined for this byte is E for error.

4 Status message gives the current value (if any) of the setting selected by the last alphabetic character sent to the 172B. If that character selects an action or a nonexistent setting, the response is a blank character.

3.6.5 Service Request Enable

"Q" followed by its argument suppresses or enables service requests. The argument may be 0 or 1. Round off is to one digit. The argument code is:

0 Suppresses all service requests.

1 Enables all service requests.

3.6.6 End of String or Terminator Specification

"X" followed by its argument designates a new End Of String (EOS), or terminator, character. The argument is the decimal value of the ASCII character that is to be the new terminator: an EOS character recognized by the 172B. Any ASCII character is accepted.

The terminator character has two uses. During output, it is appended to the end of every response to a talk request on the GPIB. During input, it signals the end of a group of programming characters. Since it is always recognized, even in a quoted string, it can be used to insure that the instrument is in a known state, so that following programming characters will be interpreted correctly.

At power on time, the EOS character is the line feed control character, ASCII character (LF) 10_{10}. When the 172B issues a talk message, the EOS character is the last byte sent. In addition, the End Or Identify (EOI) line is pulled low (END message) during the EOS character transmission. If the GPIB controller does not look for the END message (EOI line low), and it does not recognize the Line Feed (LF) as a string terminator, a new EOS character will be needed. For example, to change the EOS character from an LF to a Carriage Return (CR), program an "X13".

3.6.7 GET Mode

"O" followed by its argument selects what actions occur when a Group Execute Trigger (GET) command is sent to the 172B. The argument may be 0, 1, or −1.

0 Upon receipt of GET, the programmed waveform values are transferred to the waveform generator circuits, and then the microprocessor sends a trigger pulse if the mode is triggered or triggered haverwave. This is the same sequence of events that would occur if an Execute, then a Trigger action ("IJ") were programmed, except that no error checking is done.

1 Upon receipt of GET, the stored setting next in sequence after the last stored setting accessed is recalled if it exists (refer to paragraph 3.7.2). Then the actions described above for code 0 are performed. This is the same sequence of events that would occur if a Next Setting, an Execute and a Trigger action ("WIJ") were programmed, except that no error checking is done.

−1 Upon receipt of GET, the stored setting previous in sequence before the last stored setting accessed is recalled if it exists (refer to paragraph 3.7.2). Then the actions described for code 0 are performed. This is the same sequence of events that would occur if a Previous Setting, an Execute and a Trigger action ("UIJ") were programmed, except that no error checking is done.

3.6.8 LOCAL Key

Pressing the front panel LOCAL key switches the GPIB interface to the local mode if it is not in the local lockout mode. The "R" (remote) character on the right side of the display will go off when this key is pressed. This allows manual intervention in sequences of GPIB programming. If it is desired to totally prevent front panel alteration of the instrument's state, the GPIB interface must be put into the local lockout mode (refer to paragraph 3.6.2.4, item 4.).

3.7 STORED PROGRAMS

Up to 240 different states of the instrument can be stored in and recalled from Random Access Memory (RAM). The programs (groups of seven settings) stored in RAM are lost if instrument power is turned off. Each progrm contains information specifying instrument frequency, amplitude, offset, mode, function, symmetry and load; all other instrument settings are unaffected.

3.7.1 Storing Programs

Programs may be stored by keyboard or a command received over the GPIB interface. To store a program, first program the seven settings (frequency, amplitude, etc.) which are remembered in a program to the desired value, if not already programmed. Then press the STOR key or program the letter "M", followed by a number between 1 and 240, which identifies the particular program. The previous program with that number assigned, if there was one, is erased by the entry of the new settings. In any case, the current values of the frequency, amplitude, mode, function, symmetry and load settings are stored into the selected program. When a program is stored, the settings are tested for consistency in the same manner as with an Execute command (refer to paragraph 3.3.8). The program is always stored whether or not errors were detected.

3.7.2 Recalling Programs

The information stored in a program may be recovered either from the front panel or by a command over the GPIB. To recall from the front panel, press the RCL key, followed by the number of the desired program. When the next nonnumeric key is pressed, the seven settings stored in the selected program are transferred to the display memory and the analog scratch pad memory. Then data is available to be sent to the analog circuitry of the instrument, or, if desired, it may be examined and possibly altered by use of the front panel keys. Recalling a program over the GPIB is a similar process. First, a "Y" character is programmed, followed by the number of the desired program. When the number is terminated, the program information is transferred to the display and analog scratch pad memories, as above. To preserve compatibility with previous models, the CMD RCL key ("R") and "Z" also access stored programs, acting like the letter "Y".

The identifying numbers of programs in RAM range from 1 through 240. If the number of a program which does not exist or an illegal identifying number is programmed, an error will result.

Pressing the NEXT key or programming "W" causes the program next in sequence after the last program accessed to be recalled. This provides an automatic way to recall a sequence of programs. However, the programs need not be numbered consecutively. If there is no program following the last program accessed, an error occurs.

Pressing the LAST key or programming "U" causes the program previous in sequence before the last program accessed to be recalled. This action works like the NEXT ("W") action previously described, except that programs are recalled in descending numeric order.

3.7.3 Recalling Stored Settings for External Storage

To save existing stored instrument settings, the settings stored at each address must be recalled to the analog scratch pad memory and placed on the GPIB as a status talk message, where they may be recorded on magnetic tape or whatever.

Program a status talk message (T0). Program a recall of the first stored settings (YX where X is 1 - - - 240). Place the scratch pad memory contents on the GPIB by sending the 172B talk address with ATN on. Thereafter, program "W" to call up the next stored settings. Continue the process until all settings are transmitted. (Refer to Appendix C, example 3.)

3.7.4 Deleting Programs

To delete a program, program the letter "M" followed by a *minus* sign and the number of the program to be removed. When the number is terminated, the program is removed from storage; there is no other effect.

3.7.5 High Speed Recall

When the GET mode ("O") setting is set to either 1 or −1, a sequence of programs may be recalled in either ascending or descending order at high speed by sending Group Execute Trigger (GET) commands to the instrument (refer to paragraph 3.6.7). In this mode of operation, the next (or previous) program is recalled and executed, and the waveform circuits are triggered, all within 2 ms of receiving the GET command. (Refer to Appendix C, example 4.)

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The major components of the Model 172B are shown in figures 4-1, 4-2 and 4-3. The blocks in figure 4-3 correspond to actual assemblies. Each circuit board is shown as a block diagram in subsequent figures.

The analog portion of the 172B consists of a function generator (VCG, Triangle Generator and Function/Preamp boards), output amplifier with offset and attenuator (Attenuation board) and an optional frequency synthesizer (1st Digit/Mixer, 2nd and 3rd Digit and 4th and 5th Digit/Reference boards). The synthesizer is controlled by logic to produce some multiple of the desired output frequency; its output is within the 1 to 13 MHz range. In synthesizer mode, this frequency is divided down to the desired frequency, by logic control, at the function generator. The function generator is then phase locked to it. In function generator mode, the frequency may be controlled by VCG voltage as well as logic, and, in external phase lock mode, phase lock occurs when the 172B frequency remains within 2% of the external signal frequency.

The digital portion of the 172B consists of the bus and front panel inputs to the microprocessor (Microprocessor and Memory RAM boards) and its output to the analog portion of the 172B. The GPIB input is interfaced to the microprocessor by the GPIB board. The microprocessor also controls the front panel readout and sends status and error messages on the GPIB.

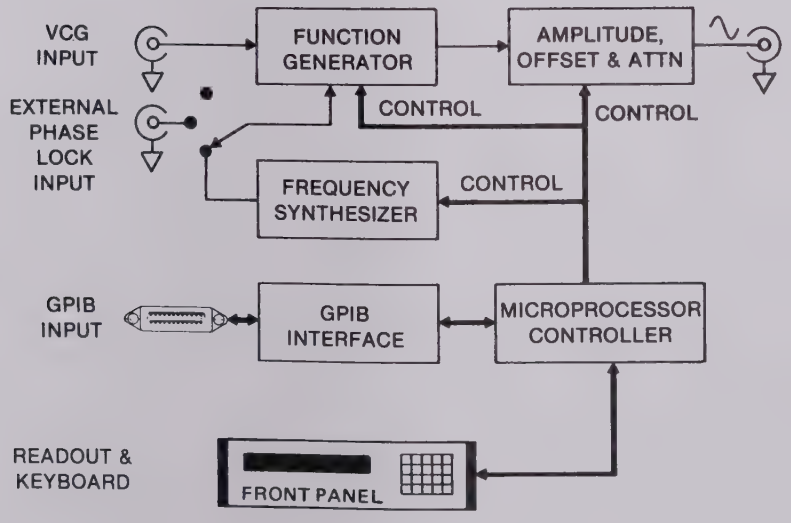
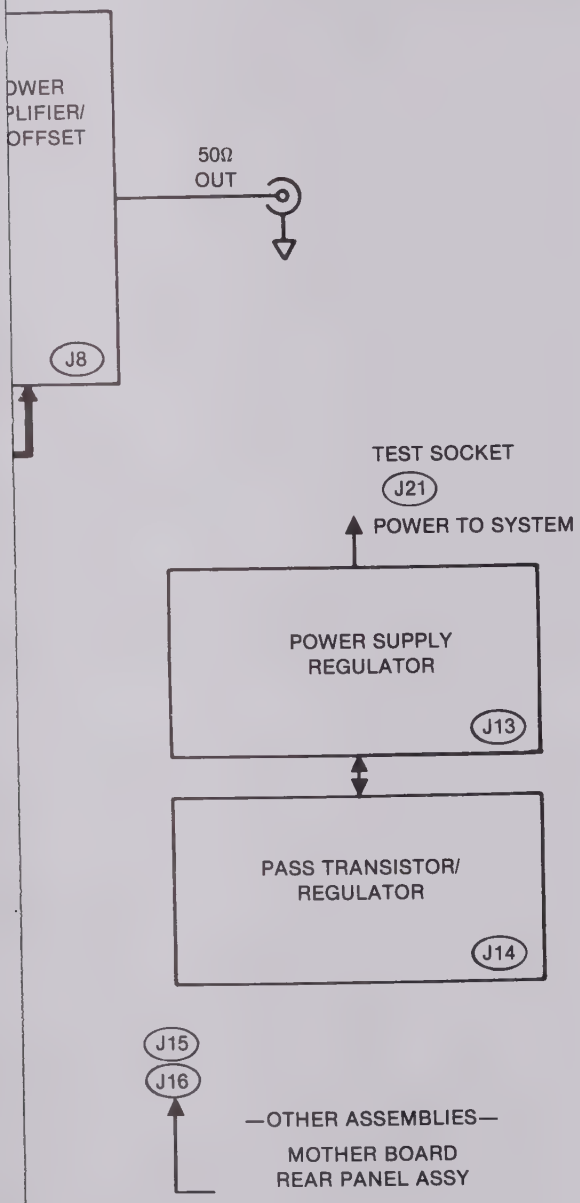
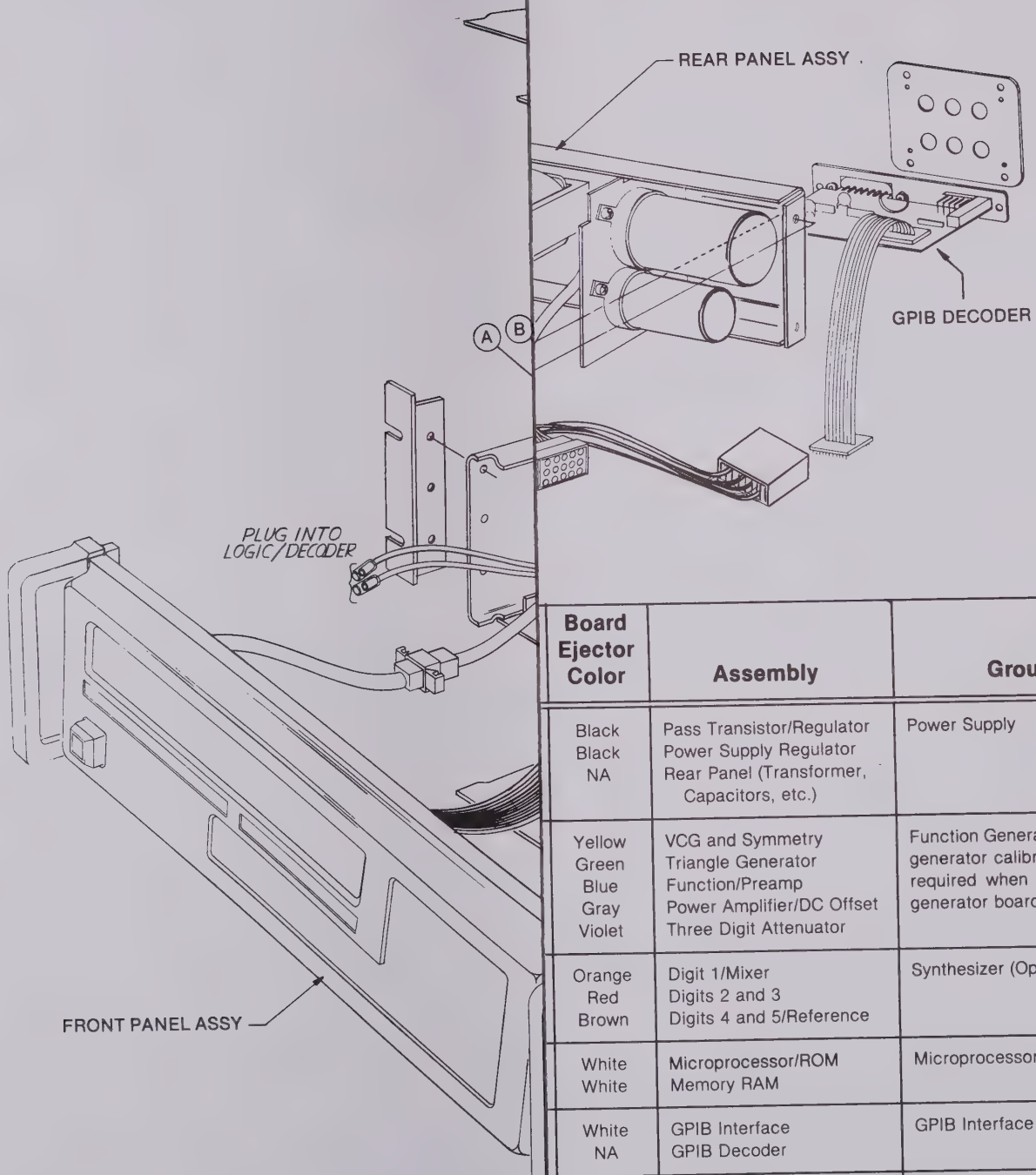


Figure 4-1. Overall Block Diagram


OWER
PLIFIER/
OFFSET
50Ω
OUT
J8
TEST SOCKET
J21
POWER TO SYSTEM
POWER SUPPLY
REGULATOR
J13
PASS TRANSISTOR/
REGULATOR
J14
J15
J16
—OTHER ASSEMBLIES—
MOTHER BOARD
REAR PANEL ASSY



Board Ejector Color	Assembly	Group
Black Black NA	Pass Transistor/Regulator Power Supply Regulator Rear Panel (Transformer, Capacitors, etc.)	Power Supply
Yellow Green Blue Gray Violet	VCG and Symmetry Triangle Generator Function/Preamp Power Amplifier/DC Offset Three Digit Attenuator	Function Generator (function generator calibration usually required when any function generator board is replaced)
Orange Red Brown	Digit 1/Mixer Digits 2 and 3 Digits 4 and 5/Reference	Synthesizer (Option 002)
White White	Microprocessor/ROM Memory RAM	Microprocessor
White NA	GPIB Interface GPIB Decoder	GPIB Interface
NA	Front Panel	Front Panel (Option 001)

Figure 4-2. Circuit Board Location

4.2 VCG AND SYMMETRY

The purpose of the VCG and Symmetry board (see figures 4-3 and 4-4) is to provide positive and negative currents to the Triangle Generator board that are proportional in amplitude to the desired three digits of frequency; and then proportional, positive current to negative current, according to the desired waveform symmetry.

The input to the VCG and Symmetry board is internal bus logic, VCG (Voltage Controlled Generator) voltage from the VCG (FM) BNC and the synthesizer signal which may be from 1 to 13 MHz, which is some power of ten multiple of the programmed frequency. The logic is controlled by programmed mode, frequency range and the three-digit frequency value.

The frequency of the generator is determined by the rate of charge and discharge of the "range" capacitance on the Triangle Generator board (see figure 4-5) by the positive and negative currents. The entire range of frequencies from 0.1 mHz to 13 MHz is achieved by selecting a capacitance, then varying the current from low to high. When near maximum current is reached, a smaller capacitance is selected and the current increased from low to high again. Each set of capacitance determines a frequency range. This scheme is used until 1 MHz is reached. From 1 through 13 MHz, an additional boost in current is used in lieu of a change in capacitance. (Symmetry control is inhibited on this range.) This boost is logic controlled (see figure 4-4), as is switching in individual alignment resistors for each range. See frequency range blocks on the diagram. Internal bus control logic from the microprocessor also selects three digits of frequency within a range and determines whether or not external voltage (VCG) will be allowed to share in the control of the frequency of the generator. If in synthesizer or phase lock mode, VCG is not allowed. The input VCG voltage, if allowed, is combined with the other voltages at the digital to analog amplifier to drive the current generators.

Programming the symmetry selects the resistances which control the balance between the positive and negative current generators.

In phase lock or synthesizer mode, the analog voltage that controls the current generators is supplemented with the error voltage required to maintain phase lock with an external signal or phase lock with the synthesizer circuits. This error voltage is generated by phase detecting the difference between the square wave from the triangle generator hysteresis switch and the external signal or the synthesizer signal, whichever was selected by mode logic. The generator square wave will be in phase with the external input and the sine wave 90° out of phase when external phase lock is selected. The external signal and the generator signal must be within 2% of frequency for phase lock to occur. The compared synthesizer frequency is always within 2% of the generator frequency. The synthesizer itself has a range of only 1 to 12.999 MHz; hence, the divide by N circuit prior to the phase detector.

If the generator frequency is in the 10^6 range, no division is required; however, for each lower range a division must occur prior to phase detection and phase locking of the generator to the synthesizer:

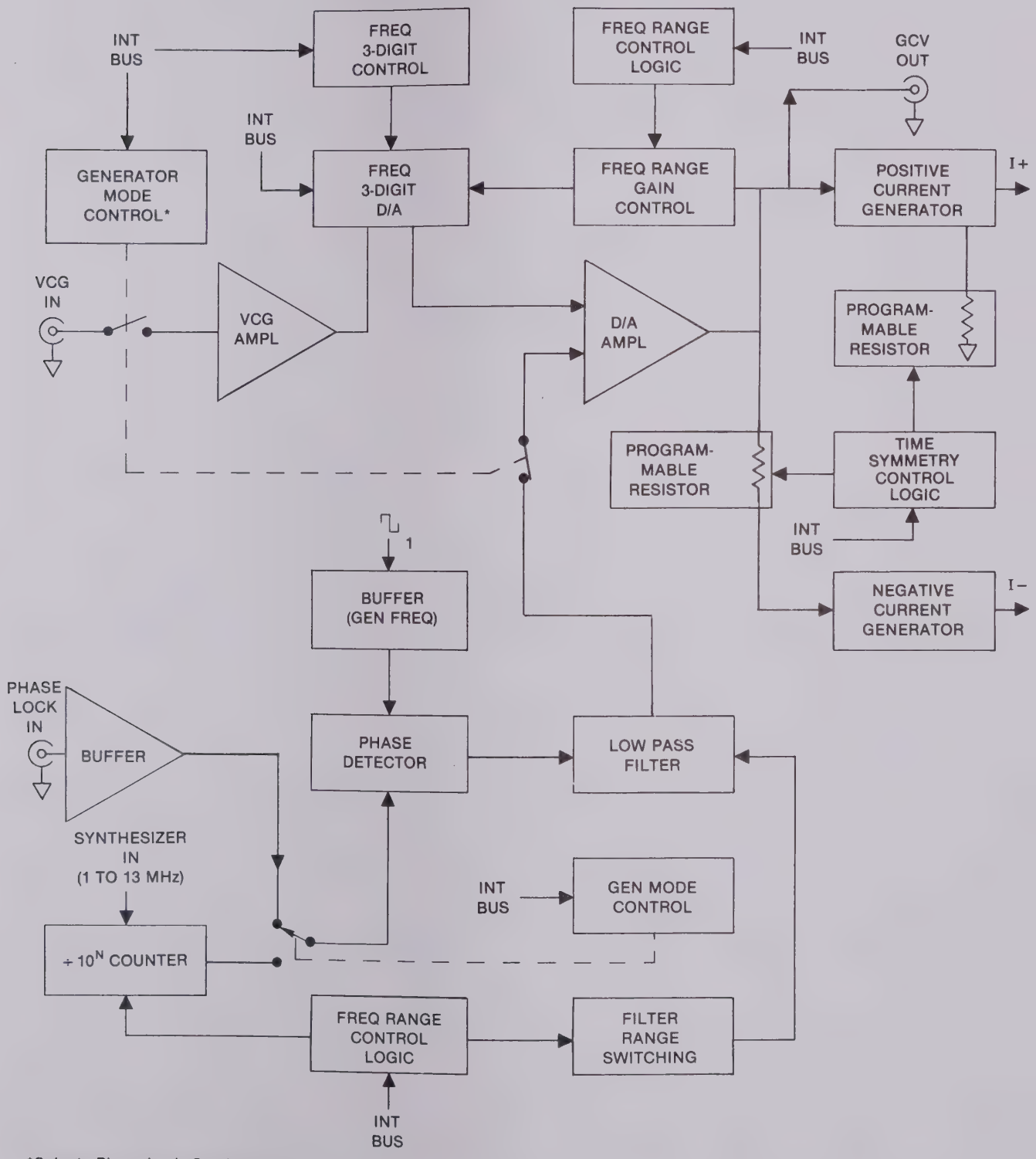
Range	N
10^6	1
10^5	10^1
10^4	10^2

etc.

The purpose of the Triangle Generator board (see figures 4-3 and 4-5) is to produce both the triangle and square waveforms at the frequency determined by the currents from the VCG and Symmetry board. The generator will free run or will turn on and off in response to a trigger or gate voltage, depending on the mode selected.

Input to the board is trigger voltage applied at the TRIG IN BNC, internal bus control logic and positive and negative currents proportional to the programmed frequency and symmetry from the VCG and Symmetry board. Output is the triangle and square waveforms to the Function/Preamp board and a sync signal based on the square wave to the SYNC OUT BNC. Triggered output starts at the normal 0° waveform phase or, when in haverwave modes, −90° phase.

The diode switch, which is controlled by the hysteresis switch, is used to switch the positive or negative current to the timing capacitor selected by the frequency range logic. When the positive current is switched into the timing capacitor, the voltage across the capacitor will rise linearly to generate the triangle rise transition. When the current is negative, the voltage across the timing capacitor will fall linearly to produce the fall transition of the triangle.



*Selects Phase Lock, Synthesizer or VCG

Figure 4-4. VCG and Symmetry Block Diagram

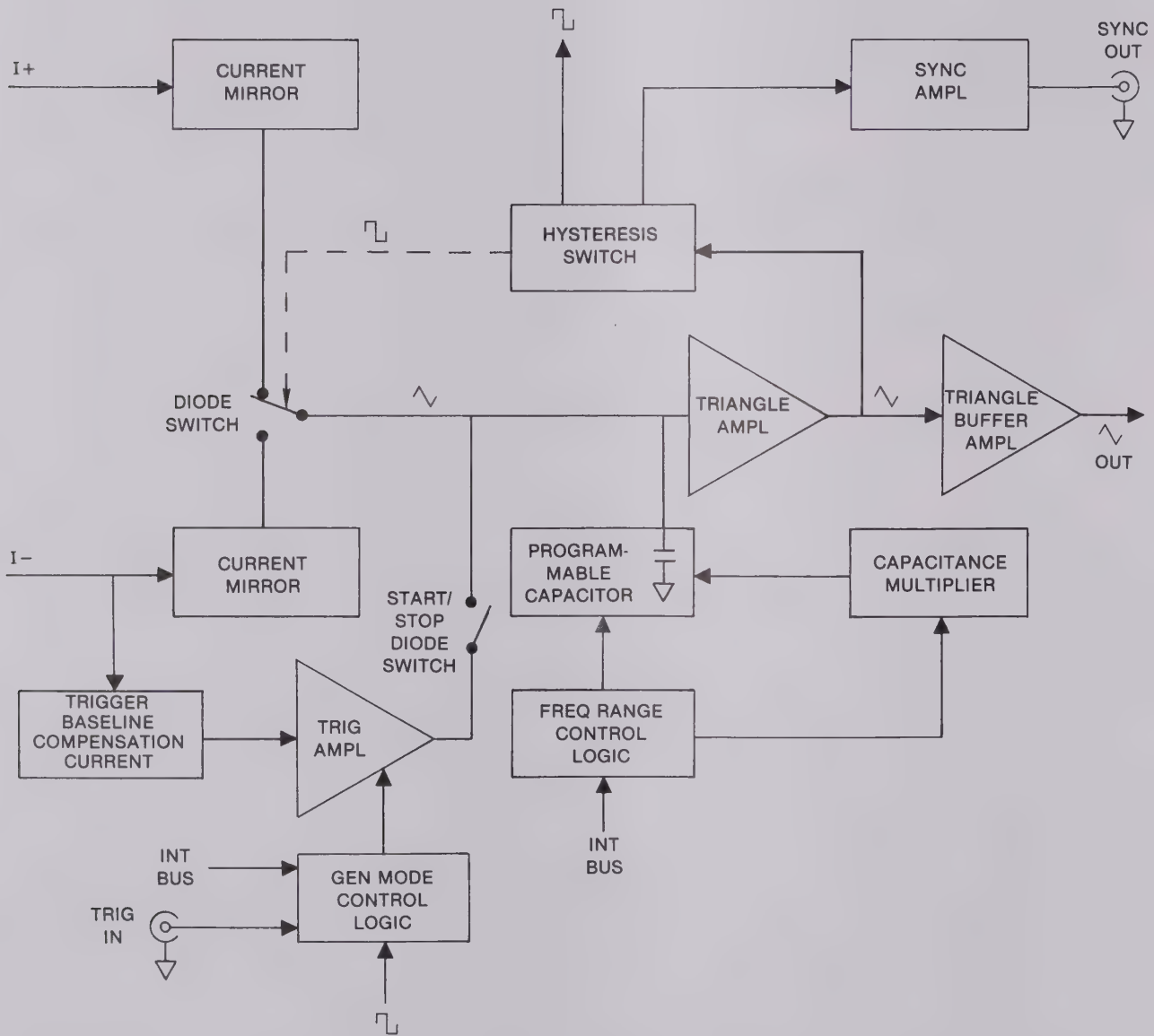


Figure 4-5. Triangle Generator Block Diagram

The triangle amplifier output is fed to the hysteresis switch and to the ^v buffer amplifier. The ^v buffer is fed to the Function/Preamp board (see figure 4-6). The hysteresis switch has two voltage limit points (+1.25 and −1.25) at its input.

During the time the output voltage of the triangle amplifier is rising, the output voltage of the hysteresis switch is positive, but when the output voltage of the triangle amplifier reaches +1.25V, it triggers the hysteresis switch, causing the hysteresis switch output to switch negative. Once the control voltage into the diode gate becomes negative, it switches the positive current out and the negative current in to the timing capacitor, so that the direction in the voltage change across the capacitor reverses, starting a linear decrease of the waveform. When the decreasing voltage reaches −1.25V, the hysteresis switch output switches back to positive, reversing the process. This action generates the triangle waveform. Since the hysteresis switch output is a square wave, the result is simultaneous generation of a square wave and a triangle wave at the same frequency.

The frequency is range controlled by selecting various capacitance and finely controlled by the charging currents. Symmetry of the waveforms is controlled by the degree of imbalance between positive and negative currents. To avoid the use of very large capacitors for the low frequency ranges, a capacitance multiplier circuit simulates a larger capacitor by a proportional decrease in charging current.

The enabling of generator operation is controlled by allowing or preventing the selected timing capacitor to charge. For continuous operation, the trigger amplifier maintains a positive level above the positive peak developed by the charging capacitors. This reverse biases (turns off) the start/stop diode switch, preventing the trigger amplifier from affecting continuous operation.

When in trigger mode, the trigger amplifier outputs some level below the positive peak charging level, the diode switch is forward biased (turned on) holding the charging level constant and preventing the capacitor from charging to the positive peak. This stops operation and holds the output at a dc level called the trigger baseline, the level from which a waveform cycle starts and where it will stop. Normally, this is midway between the peaks. In the haverwave mode and for square and pulse functions, it is at the negative peak level.

When the charging level is being held, the negative current generator still varies its output with corresponding frequency control inputs. These varying currents must be taken up through the diode switch to keep the timing capacitors from varying their charge, and thus the trigger baseline. The baseline compensation circuit monitors the output from the negative current generator to control the trigger amplifier, and thus the necessary compensating current through the diode switch.

The generator mode control circuit determines whether the trigger control logic is to be "fired" for just one cycle, or is to be held on for the duration of the trigger input during gated mode or is to be held on continuously during continuous mode. When in gated mode, the trigger signal is directly coupled for controlling the trigger control logic. In the trigger mode, the trigger signal is capacitively coupled to provide a leading edge spike to "fire" the trigger control logic. The trigger control logic determines that after a waveform starts, it always stops at a complete cycle at the same phase at which it started. The trigger control logic latches the trigger amplifier for an enabling output from the time the cycle starts to when the negative peak of the last cycle is reached (just one cycle in the trigger mode). Upon reaching the negative peak, the timing capacitor wants to continue charging positive again as usual, but stops upon reaching the trigger baseline. A square wave from the hysteresis switch synchronizes the last negative peak time for unlatching the trigger amplifier.

4.4 FUNCTION/PREAMP

The Function/Preamp board (see figure 4-3 and 4-6) creates a sine waveform and selects the output function as one of the following:

Sine wave
Triangle wave
Square wave
Inverted (with respect to sync) sine wave
Inverted (with respect to sync) triangle wave
Inverted (with respect to sync) square wave
No signal

The input to the Function/Preamp board is the buffered triangle wave and square waveform from the Triangle Generator board and the internal bus logic. Output is the selected function or dc, which goes to the Three-Digit Attenuator board (see figure 4-7).

The triangle wave is processed by nonlinear diode networks to produce a sine wave, and the square wave is precisely clipped. All three waveforms, triangle, sine and square, are present for function selection by logic. The selected waveform, or no waveform, is amplified and presented in both normal and inverted form for final logic selection.

4.5 THREE-DIGIT ATTENUATOR

The Three-Digit Attenuator board (see figures 4-3 and 4-7) accurately controls the amplitude of the output signals from the Function/Preamp board and within the particular range setting.

The input is the internal bus logic and the signal selected by the Function/Preamp board. The output is the attenuated signal sent to the Power Amplifier/DC Offset board. The logic sets the attenuation network to accurately produce an amplitude expressed as XX.X.

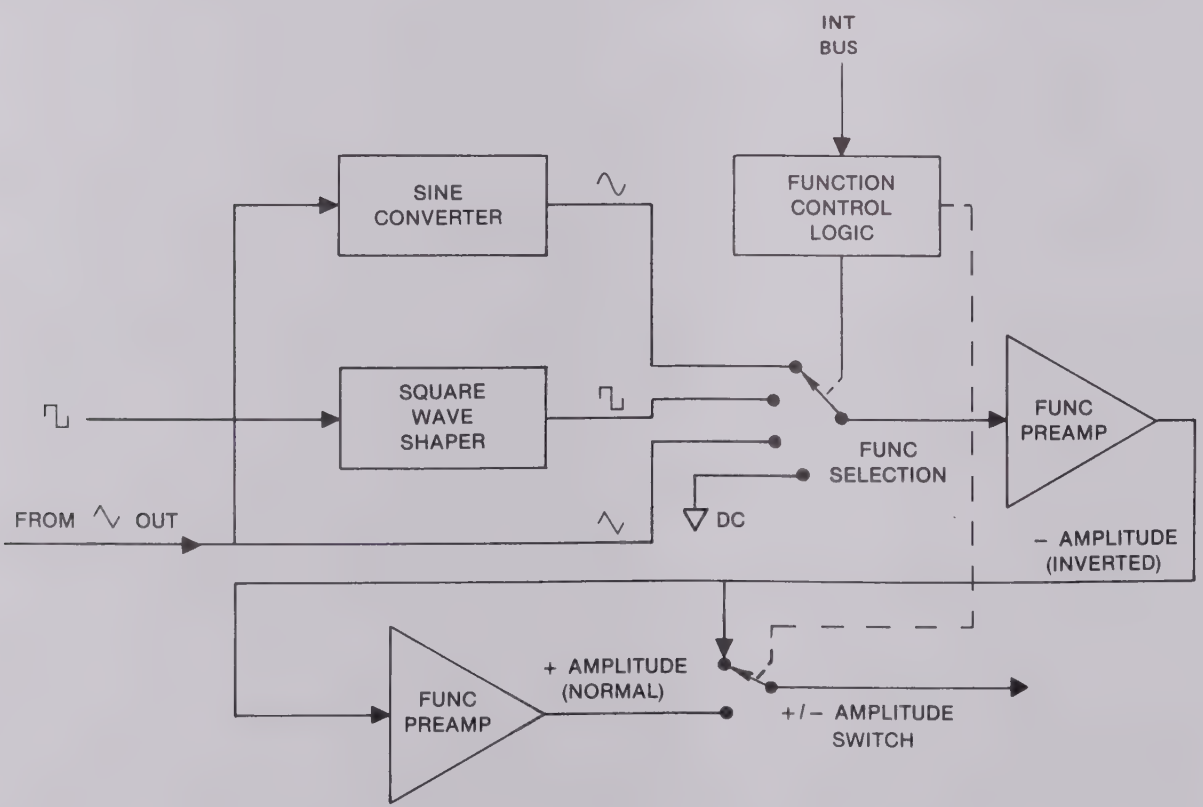


Figure 4-6. Function/Preamp Block Diagram

4.6 POWER AMPLIFIER/DC OFFSET

As controlled by logic, the Power Amplifier/DC Offset board (see figures 4-3 and 4-7) amplifies the three-digit attenuated signal by the amount corresponding to the amplitude range value; dc offsets the signal, connects or disconnects the signal from the output BNC and connects or disconnects an internal load termination. The input to the board is the three-digit accurate signal (X.XX) from the Three-Digit Attenuator board and internal bus logic. The output is the finally processed signal to the output BNC connector.

The three-digit signal is amplified and offset (if required) at the power amplifier circuit. The three-digit value of offset (X.XX) is logic controlled as is the positive or negative direction of offset. The sum of offset and signal amplitude is amplified to 15 volts peak (30V p-p), then attenuated to the logic controlled range value. The range value is logic selected to be the greater of amplitude or offset programmed range. The output signal is then output and loaded according to control logic.

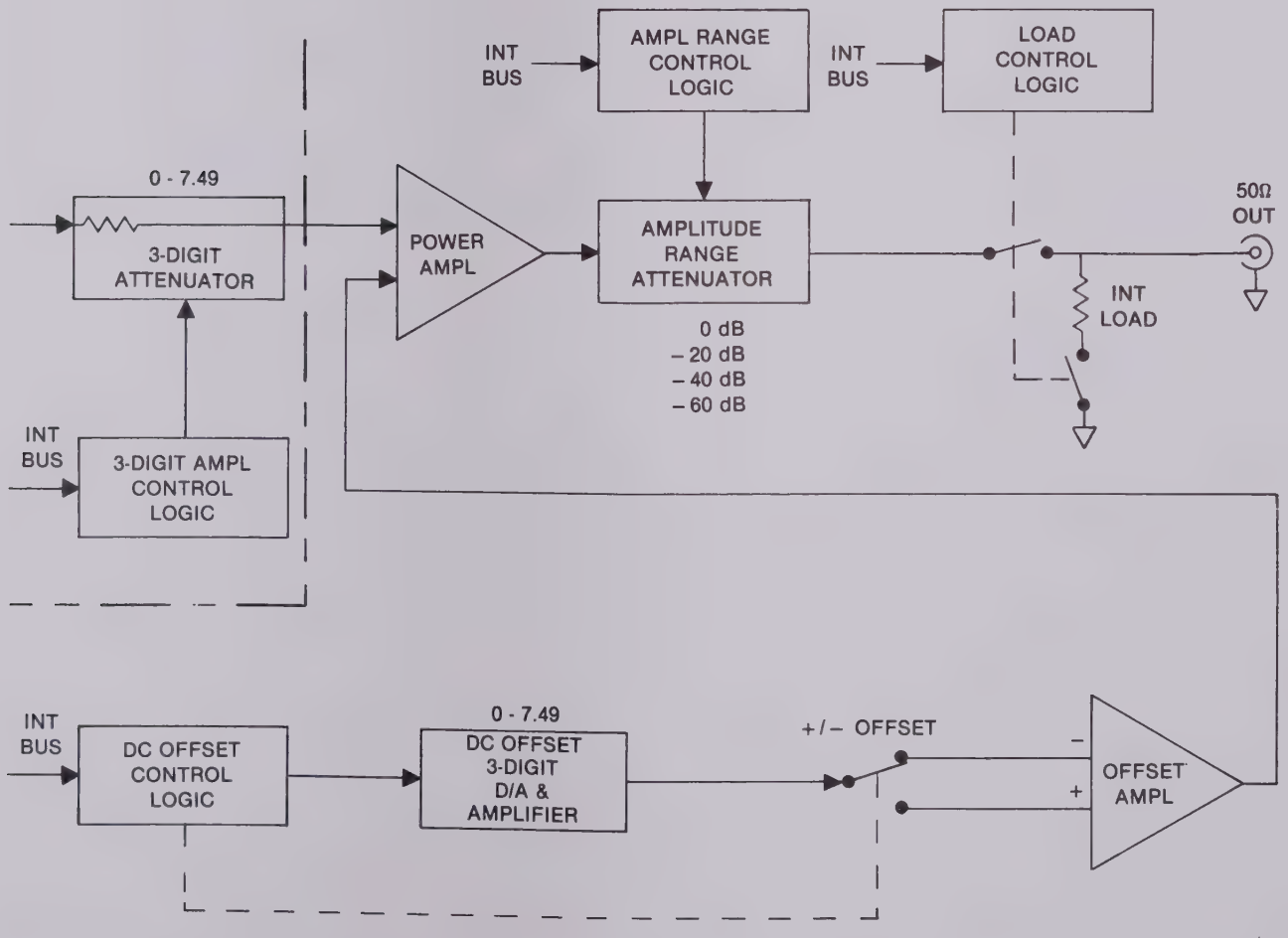


Figure 4-7. Three-Digit Attenuator and Power Amplifier/DC Offset Block Diagram

4.7 SYNTHESIZER (An Option)

The synthesizer (see figure 4-3: Digit 1/Mixer, Digits 2 and 3, Digits 4 and 5/Reference boards) provides 1 to 12.999 MHz with five-digit accuracy. The function generator circuit is phase locked to multiples of the synthesizer output for waveform functions with five-digit frequency accuracy. Four phase locked loops (PLL's) are connected together along with a mixing system and a reference section of the required fixed frequencies to make up the synthesizer. These sections are packaged as Digit 1/Mixer board, Digits 2 and 3 board and Digits 4 and 5/Reference board.

Figure 4-8 is the block diagram of a simple PLL. The output frequency is to be exactly some multiple of the reference frequency (f_r). The output frequency of the voltage controlled Variable Frequency Oscillator (VCO) is divided by a digital counter circuit. The output frequency of the divide by N($\div$ N) is compared with the reference frequency (f_r) by a frequency phase detector. If the frequency and/or phase of the two signals differ, an error voltage is generated which causes the VCO to change its frequency, moving in the proper direction to correct for the error. There is an integrator/Low Pass Filter (LPF) between the phase detector output and the VCO to eliminate high frequencies out of the detector and to insure loop stability. The output frequency is the reference frequency multiplied by the $\div$ N ratio.

Figure 4-9 is a block diagram of the digit 1 PLL of the five-digit synthesizer. The output of this loop goes from 35 to 47 MHz, as the most significant digit of the synthesizer output frequency is varied from 0 to 12 MHz. This block diagram is different from figure 4-8 in that there is a fixed $\div$ 2 ahead of the programmable divider. This makes the total $\div$ N ratio twice that of the programmable divider alone. If the total synthesizer output is required to be 10,000 MHz, then the digit 1 loop output will be 45 MHz. The number 10 will be loaded into the programmable divider in Binary Coded Decimal (BCD) form by the logic interface portion of the 172B. The programmable divider translates this number 10 into the divider ratio 45 with a PROM look-up table. The programmable divider ratio 45, together with the fixed divide by 2, gives a total $\div$ N of 90. The 500 kHz reference frequency multiplied by 90 gives an output frequency of 45 MHz. The programmable divider alone, and a 1 MHz reference frequency, would give the same results; the $\div$ 2 is used to allow a lower maximum operating frequency for the programmable divider.

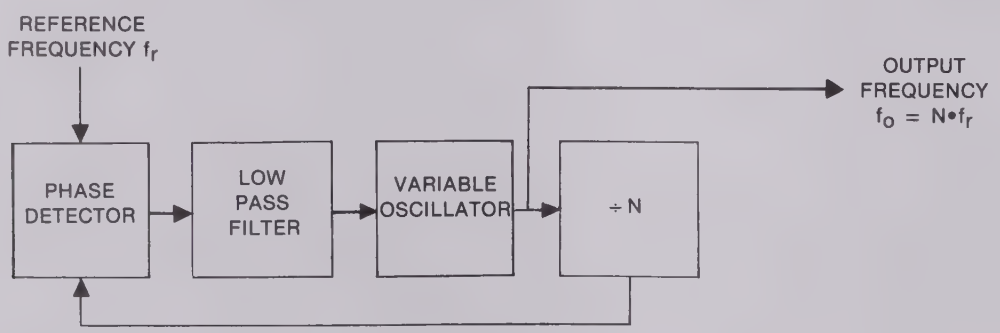


Figure 4-8. Simple Phase Lock Loop Block Diagram

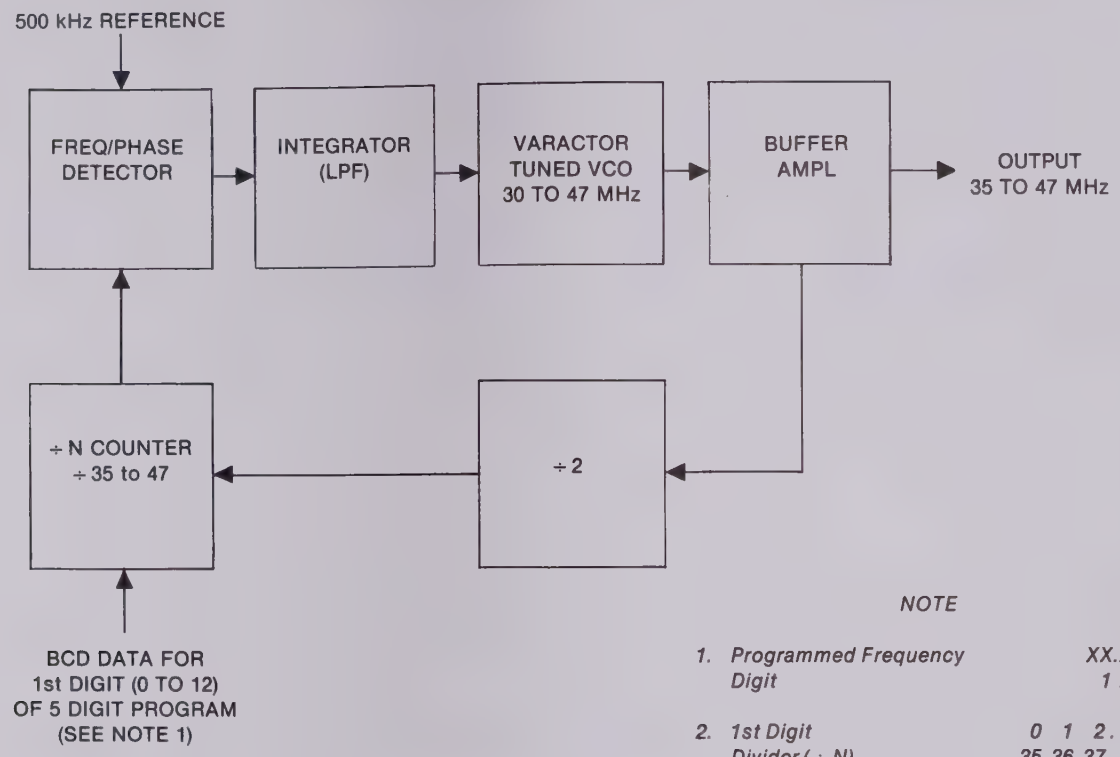

500 kHz REFERENCE
FREQ/PHASE DETECTOR
INTEGRATOR (LPF)
VARACTOR TUNED VCO 30 TO 47 MHz
BUFFER AMPL
OUTPUT 35 TO 47 MHz
÷ N COUNTER ÷ 35 to 47
÷ 2
BCD DATA FOR 1st DIGIT (0 TO 12) OF 5 DIGIT PROGRAM (SEE NOTE 1)
NOTE
1. Programmed Frequency XX.XXXX
Digit 1 2345
2. 1st Digit 0 1 2.... 12
Divider (÷ N) 35 36 37.... 47
Output (MHz) 35 36 37.... 47

Figure 4-9. Digit 1 PLL (Part of Digit 1/Mixer Board) Block Diagram

Figure 4-10 shows a slightly more complex PLL. In this loop, the VCO output is translated to a different frequency range before being divided by the ÷N counter. A bandpass filter follows a mixer to select either the resulting sum or difference frequency. This form of loop causes the VCO output to be different from N times the reference frequency by a fixed offset. Mathematically expressed, $f_O = Nf_r \pm f_m$.

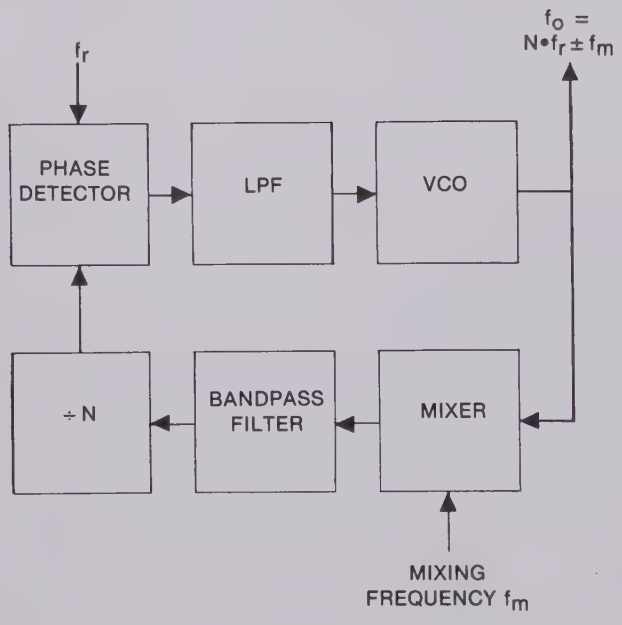


Figure 4-10. PLL With Mixer Block Diagram

Figure 4-11 shows the block diagram for digits 4 and 5 PLL. A fixed frequency of 60.0 MHz from the reference subsection is mixed with the 40 to 50 MHz VCO. The difference frequency (10 to 20 MHz) is passed through a 30 MHz low pass filter into a buffer amplifier. The amplified signal drives the divide by N counter, which divides the input frequency by a number ranging from 100 to 199, depending on the frequency setting of digits 4 and 5. The ÷N output is compared with a 100 kHz signal from the reference board in the phase detector. If there is a phase error, the phase detector will output a voltage pulse to the integrator which will change its output in the proper direction to reduce the VCO frequency error towards zero. The 4.01 to 50 MHz VCO output is divided by 100 to provide the desired 401 to 500 kHz output. The final 401 to 500 kHz output varies in 1 kHz steps as the ÷N ratio varies from 100 to 199. To obtain 500 kHz out, the required VCO frequency is 50 MHz. This mixes with the 60.0 MHz reference to produce a 10.0 MHz difference frequency. Digits 4 and 5 will both be zero in the case of a 500 kHz output, so the ÷N ratio will be 100. Dividing 10 MHz difference frequency by 100 will produce 100 kHz to compare with the 100 kHz reference. If digits 4 and 5 are set to 99, the ÷N becomes 199, and the VCO will be forced to 40.1 MHz, which will mix with 60 MHz to produce a 19.9 MHz difference frequency. The 40.1 MHz VCO will be divided by 100 to form the 401 kHz output.

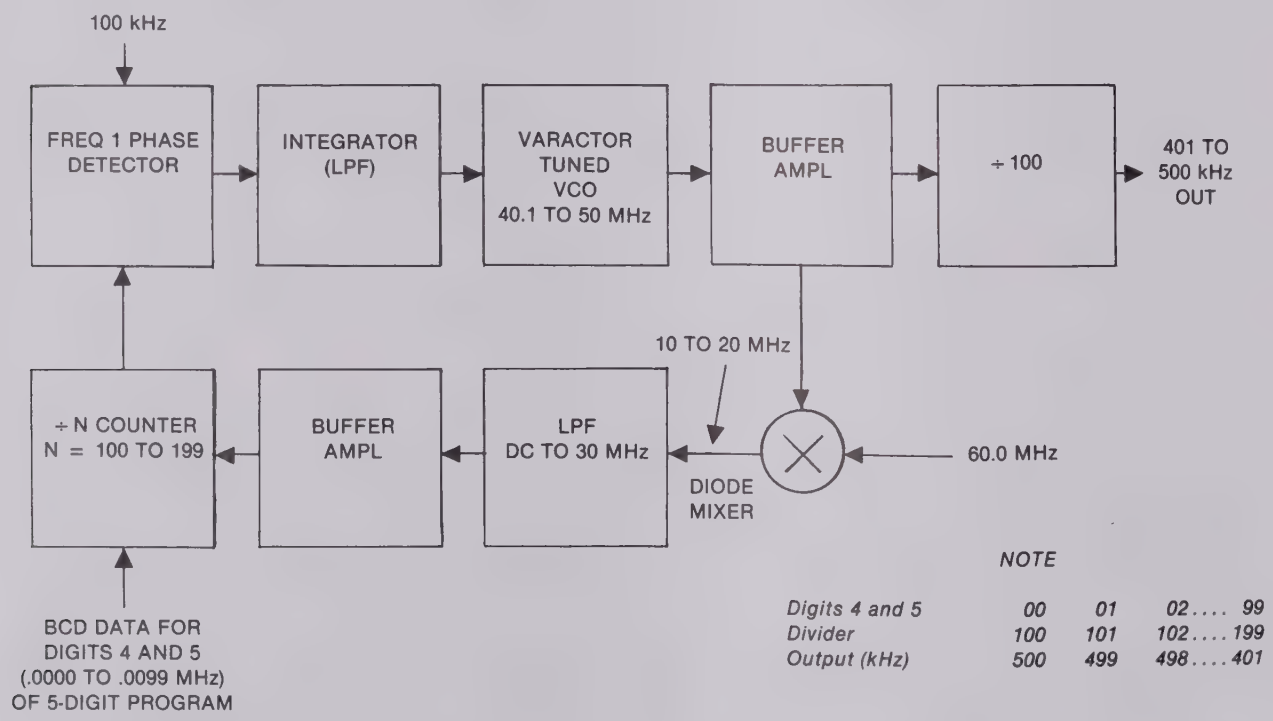
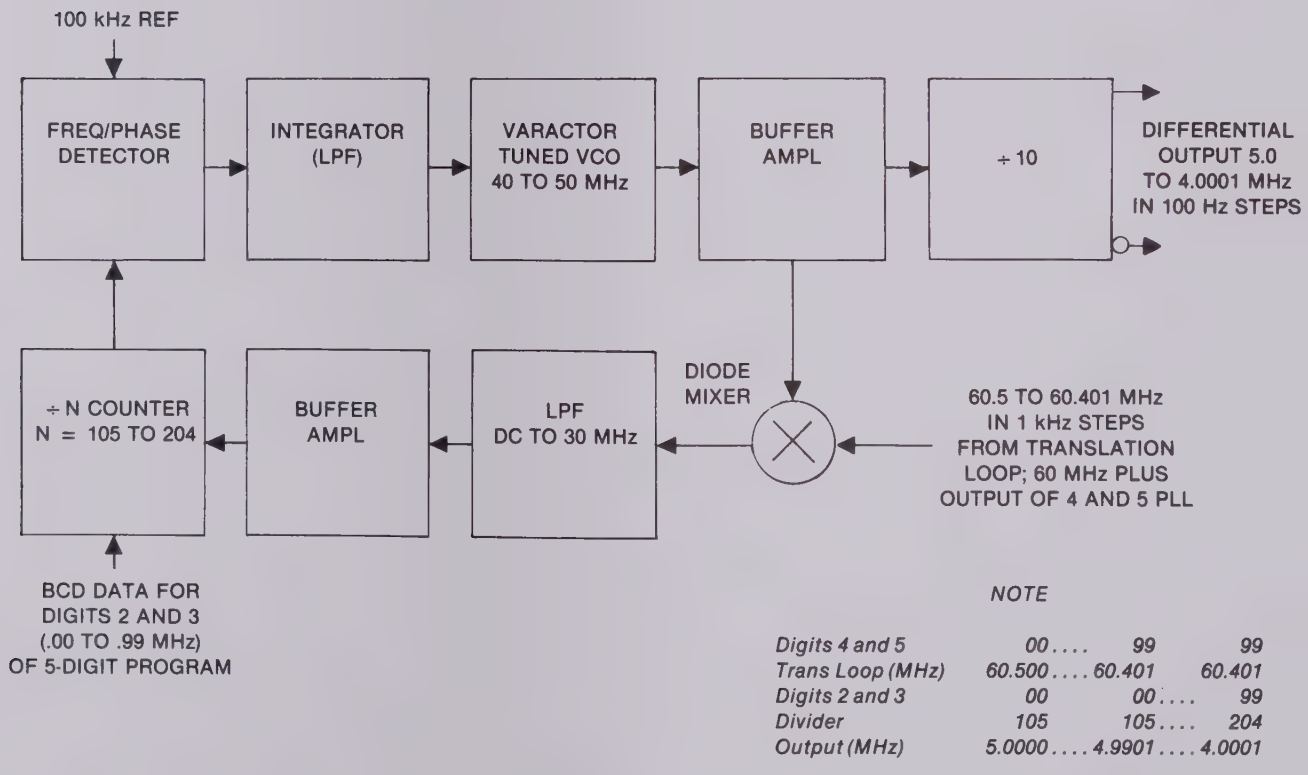

100 kHz
FREQ 1 PHASE DETECTOR
INTEGRATOR (LPF)
VARACTOR TUNED VCO 40.1 TO 50 MHz
BUFFER AMPL
÷ 100
401 TO 500 kHz OUT
10 TO 20 MHz
÷N COUNTER N = 100 TO 199
BUFFER AMPL
LPF DC TO 30 MHz
DIODE MIXER
60.0 MHz
BCD DATA FOR DIGITS 4 AND 5 (.0000 TO .0099 MHz) OF 5-DIGIT PROGRAM
NOTE
Digits 4 and 5 00 01 02.... 99
Divider 100 101 102.... 199
Output (kHz) 500 499 498.... 401

Figure 4-11. Digits 4 and 5 PLL (Part of Digits 4 and 5/Reference Board) Block Diagram

Figure 4-12 shows the digits 2 and 3 PLL. This loop is almost identical to the digits 4 and 5 PLL. The offset frequency is 60.401 to 60.500 MHz instead of 60.0 MHz and the ÷N counter ratio varies between 105 to 204 instead of 100 to 199. The VCO output is divided by 10 instead of 100, to form a 4 to 5 MHz output. If digits 4 and 5 are 00, the translation loop output to this loop will be 60.500 MHz. If digits 2 and 3 are 00, the ÷N ratio is 105. Under these conditions, the required VCO frequency is 50.0 MHz. This mixes with 60.5 MHz to produce a 10.5 MHz difference, which is divided by 105 in the ÷N to give a 100 kHz signal for the phase detector. Thus, the final output, after division, will be 5.0000 MHz. If digits 4 and 5 are set to 99, the translation loop output is 60.401 MHz. In this case, the VCO output has to be 49.901 MHz to satisfy the loop conditions, and the final output will be 4.9901 MHz. If digits 2 and 3 are also set for 99, the ÷N ratio will be 204, and a 40.001 MHz signal will be required from the VCO to mix with the 60.401 MHz to produce the 20.400 MHz difference frequency into the ÷N. In this case, the final output will be 4.0001. Thus, the output of this loop is seen to track changes in digits 4 and 5, as well as digits 2 and 3, which control the loop directly.


100 kHz REF
FREQ/PHASE DETECTOR
INTEGRATOR (LPF)
VARACTOR TUNED VCO 40 TO 50 MHz
BUFFER AMPL
÷10
DIFFERENTIAL OUTPUT 5.0 TO 4.0001 MHz IN 100 Hz STEPS
÷N COUNTER N = 105 TO 204
BUFFER AMPL
LPF DC TO 30 MHz
DIODE MIXER
60.5 TO 60.401 MHz IN 1 kHz STEPS FROM TRANSLATION LOOP; 60 MHz PLUS OUTPUT OF 4 AND 5 PLL
BCD DATA FOR DIGITS 2 AND 3 (.00 TO .99 MHz) OF 5-DIGIT PROGRAM

NOTE

Digits 4 and 5	*00*	*99*	*99*
Trans Loop (MHz)	*60.500*	*60.401*	*60.401*
Digits 2 and 3	*00*	*00*	*99*
Divider	*105*	*105*	*204*
Output (MHz)	*5.0000*	*4.9901*	*4.0001*

Figure 4-12. Digits 2 and 3 PLL (Part of Digits 2 and 3 Board) Block Diagram

Figure 4-13 is a block diagram of the translation loop. Its function is to produce a signal 60 MHz higher than the 401 to 500 kHz signal from digits 4 and 5 PLL (i.e., 60.401 to 60.500 MHz). In this loop there is no divide by N. The VCO output is mixed with a 60.0 MHz reference frequency and the difference frequency is selected by a low pass filter, buffered and applied directly to the frequency phase detector for comparison with the digits 4 and 5 output. The phase detector output drives the integrator to a voltage which sets the VCO to the proper frequency.

Figure 4-14 shows the mixer subsection and how the different loops connect together. As previously described, the digits 4 and 5 loop output is shifted upward to 60.401 to 60.500 MHz to drive the digits 2 and 3 loop. The output of the 2 and 3 loop varies from 4.0001 to 5.0000 MHz as a function of digits 2, 3, 4 and 5. This output is mixed with a 30.0 MHz signal in a double balanced modulator, and the sum of the two signals is selected by a 34 to 35 MHz bandpass filter. The output of this filter is mixed with the digit 1 loop output, 35 to 47 MHz, in a diode mixer and the difference frequency selected by a low pass filter. Take a frequency of 12.3456 MHz as an example. Digits 4 and 5 are set to 5 and 6, respectively. The output of the digits 4 and 5 PLL will be 444 kHz, and the translation loop will shift this up to 60.444 MHz. Digits 2 and 3 are set to 3 and 4; therefore, the output of the digits 2 and 3 PLL will be 4.6544 MHz, and, after mixing with 30.0 MHz, this will be 34.6544 MHz. Digit 1 is 12, so the output of the digit 1 PLL will be 47 MHz. This 47 MHz is mixed with 34.6544 and the difference is taken to form a 12.3456 MHz signal. This is the synthesizer section output which is then passed to the function generator. If the generator is set to the 1 to 13 MHz range, the function generator is phase locked directly to this signal. If the generator is on a lower range, the synthesizer output is divided by some power of 10 before the generator is locked to it.

Figure 4-15 is the block diagram of the reference subsystem. All reference frequencies are derived from a single, high stability, 10 MHz crystal controlled oscillator. This signal is multiplied by 3 to produce the 30 MHz reference, and this is then multiplied by 2 to form the 60 MHz reference. The 10 MHz is also divided by 20 to form a 500 kHz digital signal and this is divided by 5 to form a 100 kHz reference. If it is necessary to lock the synthesizer to an external 10 MHz system clock, the external clock is fed to a level detector/buffer amplifier. The output of the buffer amplifier and the internal 10 MHz oscillator are both fed to a phase detector, which in turn is fed to an integrator/low pass filter. If the external clock input is greater than 1 volt, a relay is closed automatically, connecting the integrator output to a variable capacitor for fine tuning the crystal oscillator. This locks the internal oscillator to the external system clock.

The block diagrams of figures 4-16 through 4-18 are printed circuit board oriented, showing which functions are related to what boards.

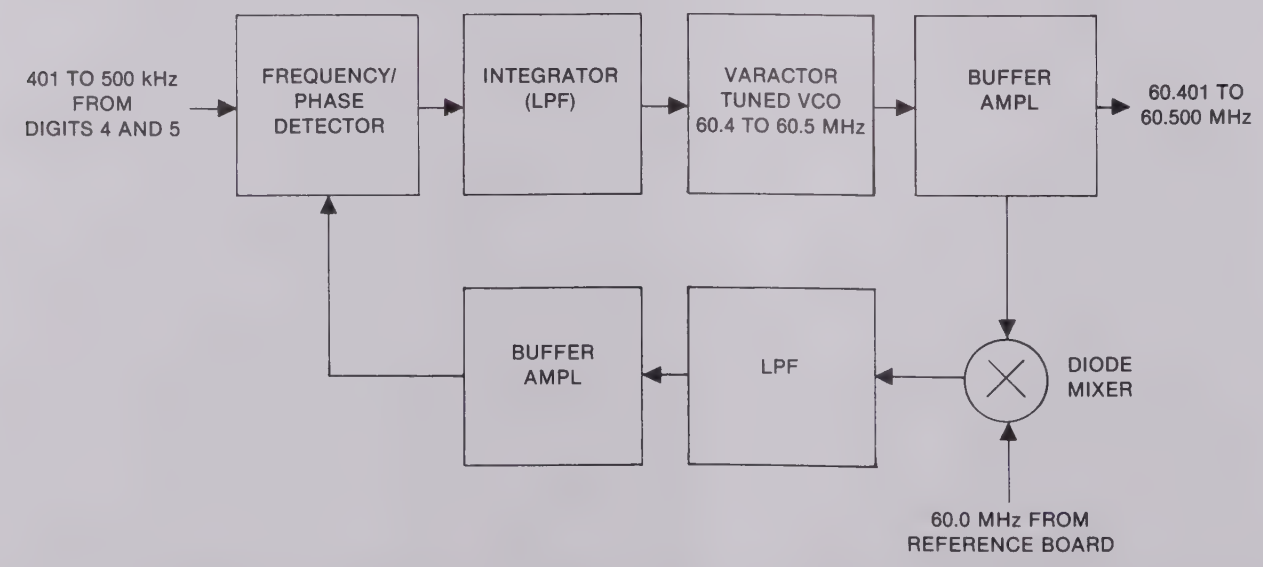


Figure 4-13. Translation Loop (Part of Digits 2 and 3 Board) Block Diagram

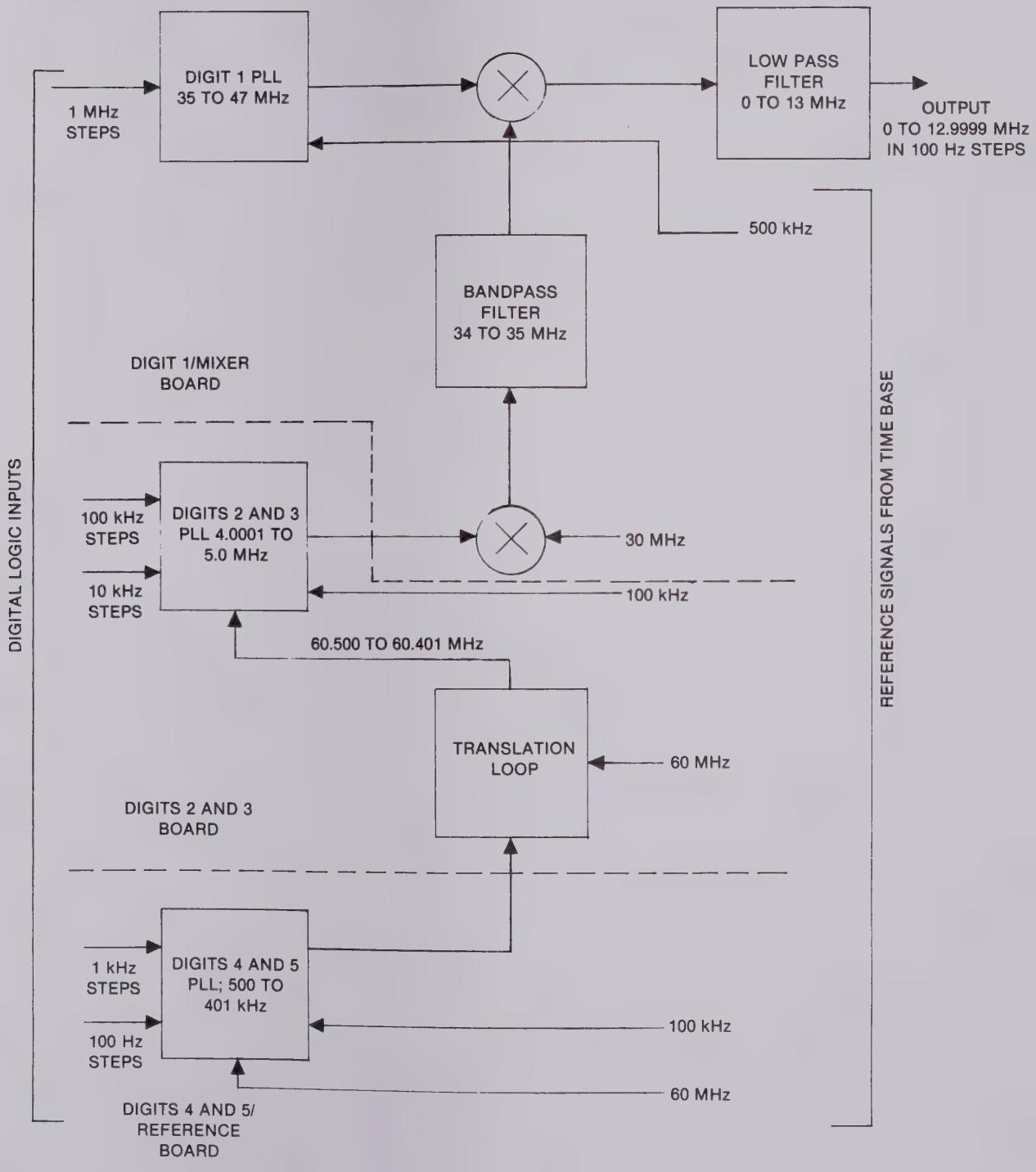


Figure 4-14. Synthesizer Block Diagram

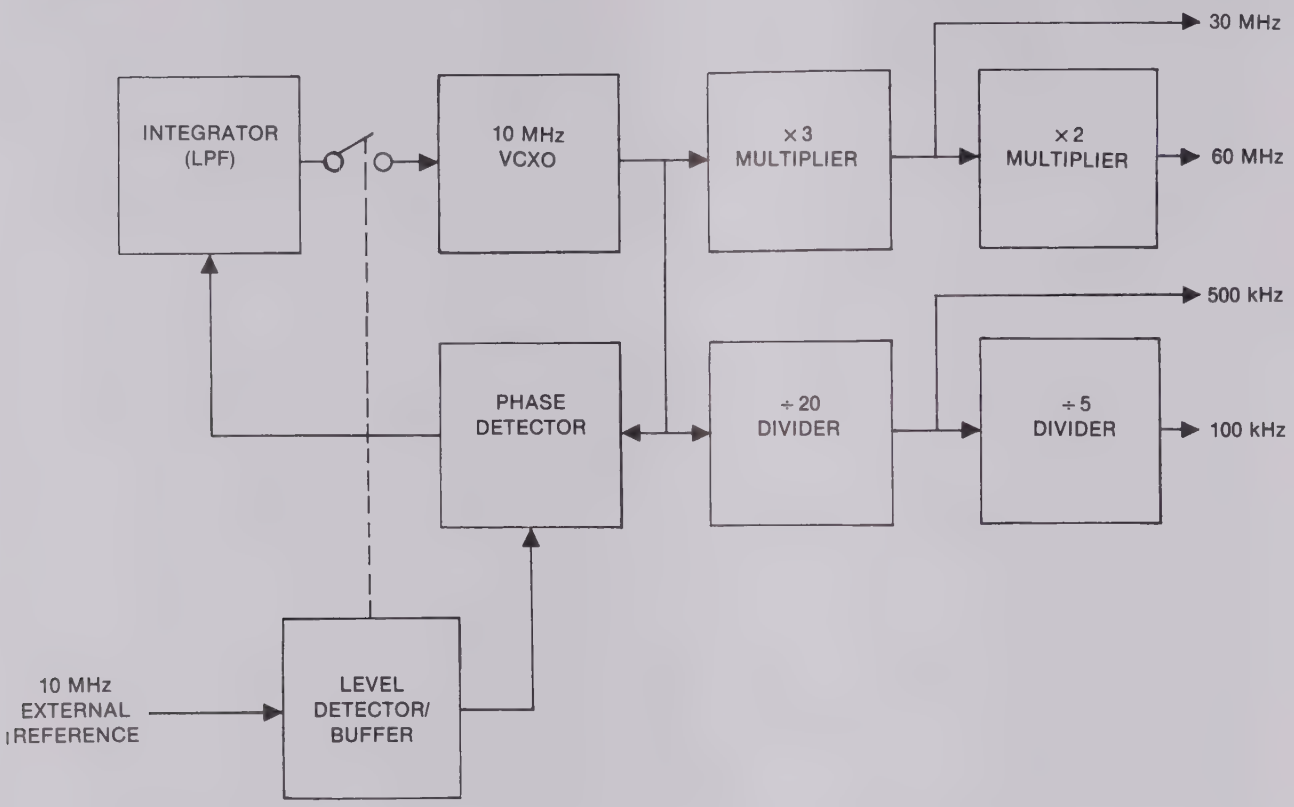


Figure 4-15. Reference Subsystem (Part of Digits 4 and 5/Reference Board) Block Diagram

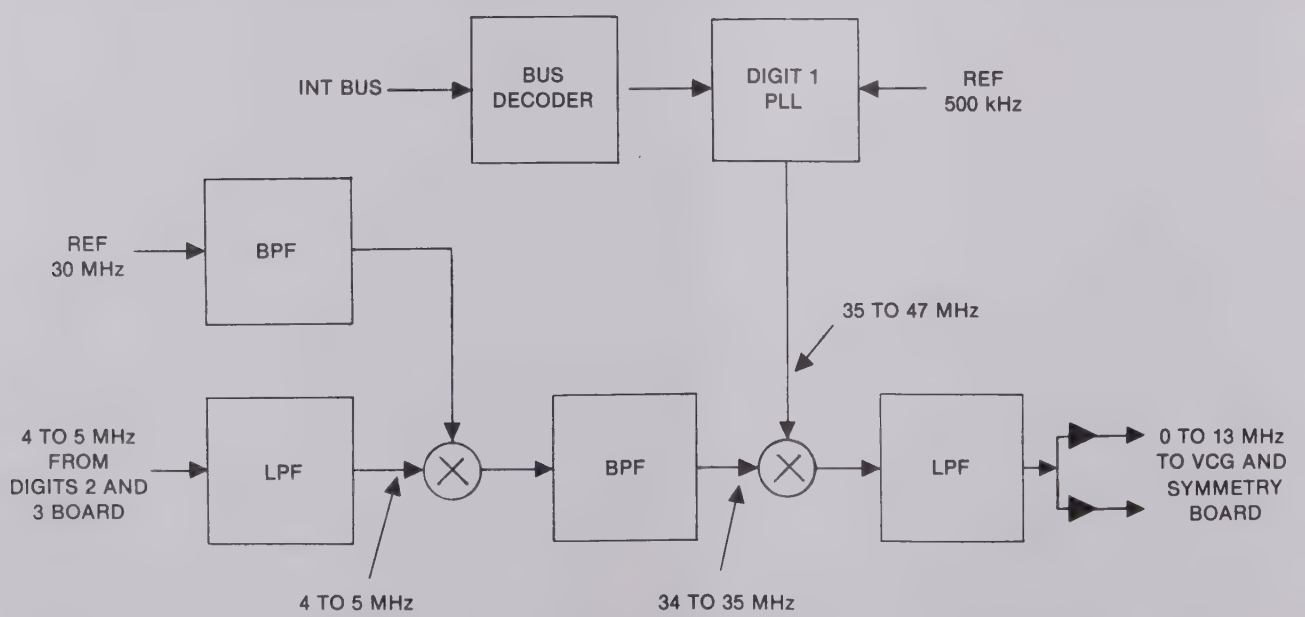


Figure 4-16. Digit 1/Mixer Block Diagram

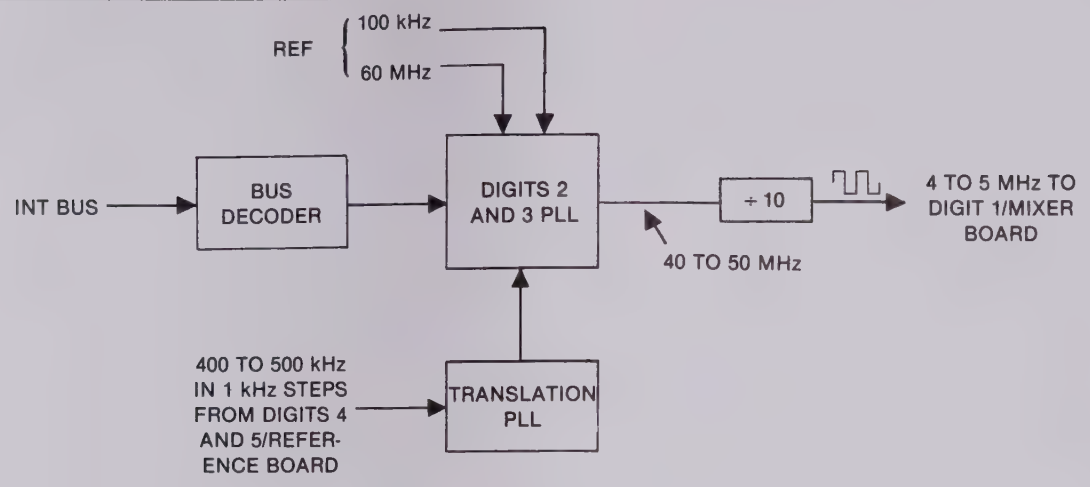

REF
100 kHz
60 MHz
INT BUS
BUS DECODER
DIGITS 2 AND 3 PLL
÷ 10
4 TO 5 MHz TO DIGIT 1/MIXER BOARD
40 TO 50 MHz
400 TO 500 kHz IN 1 kHz STEPS FROM DIGITS 4 AND 5/REFERENCE BOARD
TRANSLATION PLL

Figure 4-17. Digits 2 and 3 Block Diagram

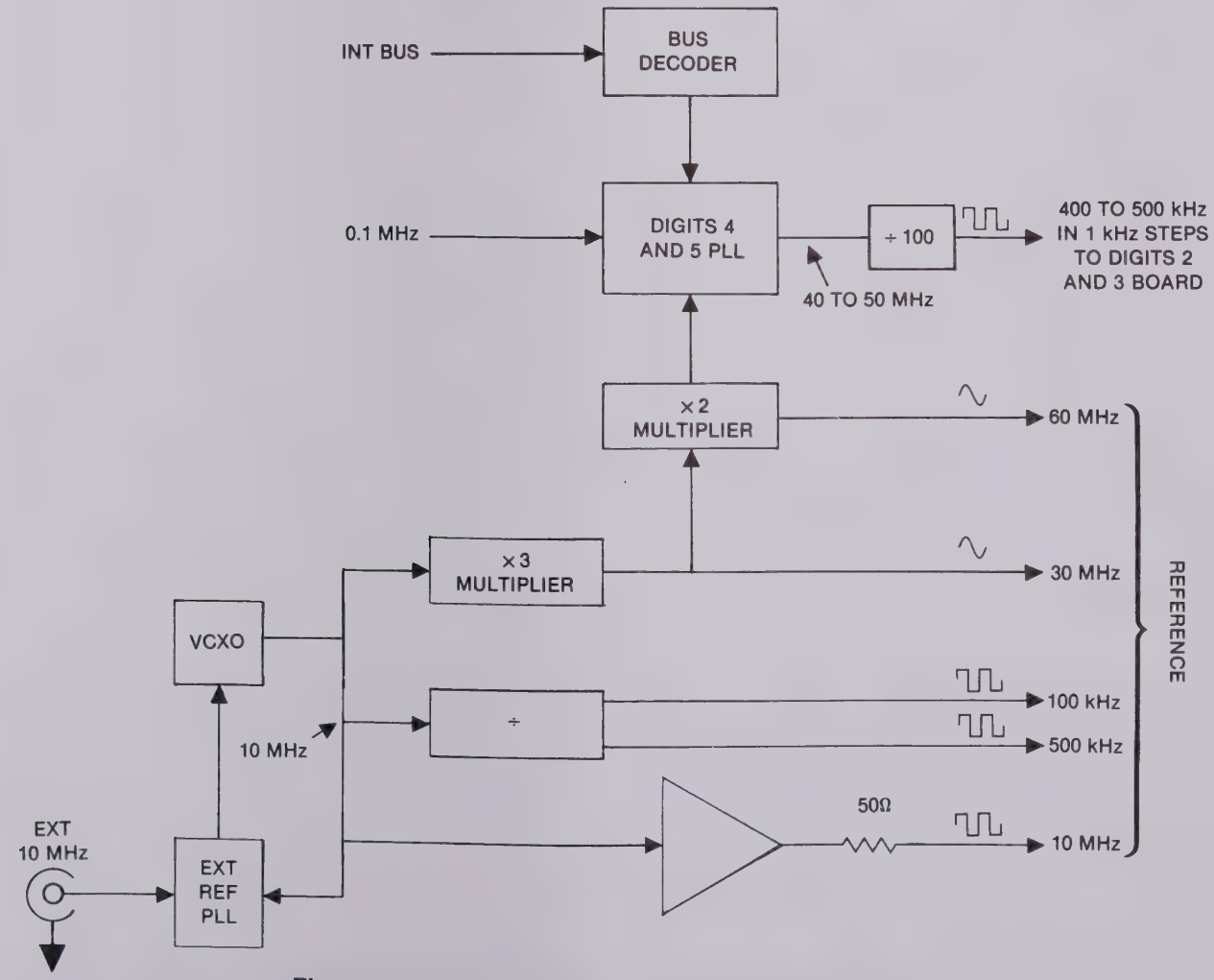


Figure 4-18. Digits 4 and 5/Reference Block Diagram

4.8 FRONT PANEL OPTION

The front panel (Option 001) contains a 46 key keyboard and a 40 character alphanumeric display to allow the user to manually program the 172B and to learn its status under both manual and remote programming. The front panel also contains the power on/off switch. The front panel assembly is connected electrically by two cables. One cable is on the power switch and can be disconnected near the front panel. The other cable carries the keyboard and display signals and is plugged into the mother board at connector J20. The front panel assembly consists of three subassemblies: the keyboard, the self-scan display and a PC board which interfaces to the microprocessor in the 172B. The microprocessor accesses the keyboard and display just as if they were read and write memory locations.

4.8.1 Keyboard

The keyboard itself consists of 46 printed circuit switches arranged in a 6×8 crosspoint array. The keyboard matrix is scanned by a keyboard encoder chip. When a contact closure is detected, the encoder stops scanning, provides a delay for contact bounce, latches a binary code onto its data output lines and provides a data ready strobe pulse. The output data is a binary number between 0 and 63 corresponding to the key depressed. When the keyboard contact closure is released, the encoder resumes scanning for the next closure. Periodically, the microprocessor, under program control, reads the encoder data output lines. The keyboard address is decoded on the microprocessor board and brought to the front panel as the keyboard out line. When this line is true, the encoder output is gated onto the 172B data bus lines, to be read by the microprocessor. The data ready strobe also triggers a 100 ms, 3 kHz audible tone each time a key is depressed.

4.8.2 Display

The display is a gas discharge device consisting of seven rows common to all character spaces, and 283 columns which are enabled consecutively, to display 40 characters on a 5×7 dot matrix, with two blank columns between characters. The display consists of a display panel and a driver board.

The information displayed on the front panel is stored in a Random Access Memory (RAM) located on the front panel PC board. Each character location on the display has a separate memory address into which the microprocessor can write. The six lower order address lines from the 172B address bus are used by the RAM as the display space addresses 0 through 39; the higher order address bits are decoded on the microprocessor board and brought to the front panel as the display enable line. When this line is true, the word appearing on the data lines 0 through 5 is written into RAM at the address appearing on corresponding address lines. Whenever the RAM is not being written into, its contents are being read to the display. The display requires a 20 kHz clock signal, valid data inputs for each particular character space, as that space is being scanned, and scan disable and reset signals to start each scan of the panel.

4.9 MICROPROCESSOR (Microprocessor and Memory RAM Boards)

The microprocessor (see figure 4-19) acts as the central processing unit, receiving information from the GPIB, the keyboard and the 172B subsystems and acting on these inputs as dicated by the software. Software directs the processor to address the subsystems and issue commands and data which direct the 172B to output the desired signals.

Software refers to a sequence of commands executed by the internal microprocessor. This sequence of instructions stored in ROM commands the microprocessor to perform according to the 172B specification. The microprocessor is powerless without a program to run; therefore, the software is one of the most vital elements of the digital section. All information transfer takes place under the control or supervision of the software. Programs are composed of machine language instructions, messages and tables that provide sequencing information.

Program data from the ROM temporary data from the RAM and input data from the keyboard or GPIB are hooked up to the microprocessor through an interconnection bus on the mother board. Data from the microprocessor software is sent to the rest of the instrument via a scratch pad memory. Table 4-1 indicates the format of the contents of the scratch pad.

The two boards of the microprocessor section (microprocessor and memory RAM) may be installed in locations C, D or E (see figure 4-1). The cards receive and drive a 43 wire data bus terminated on the mother board.

4.9.1 Microprocessor Board

This board contains an eight bit processor, software in ROM, buffers, decoders and two I/O ports. Figure 4-19

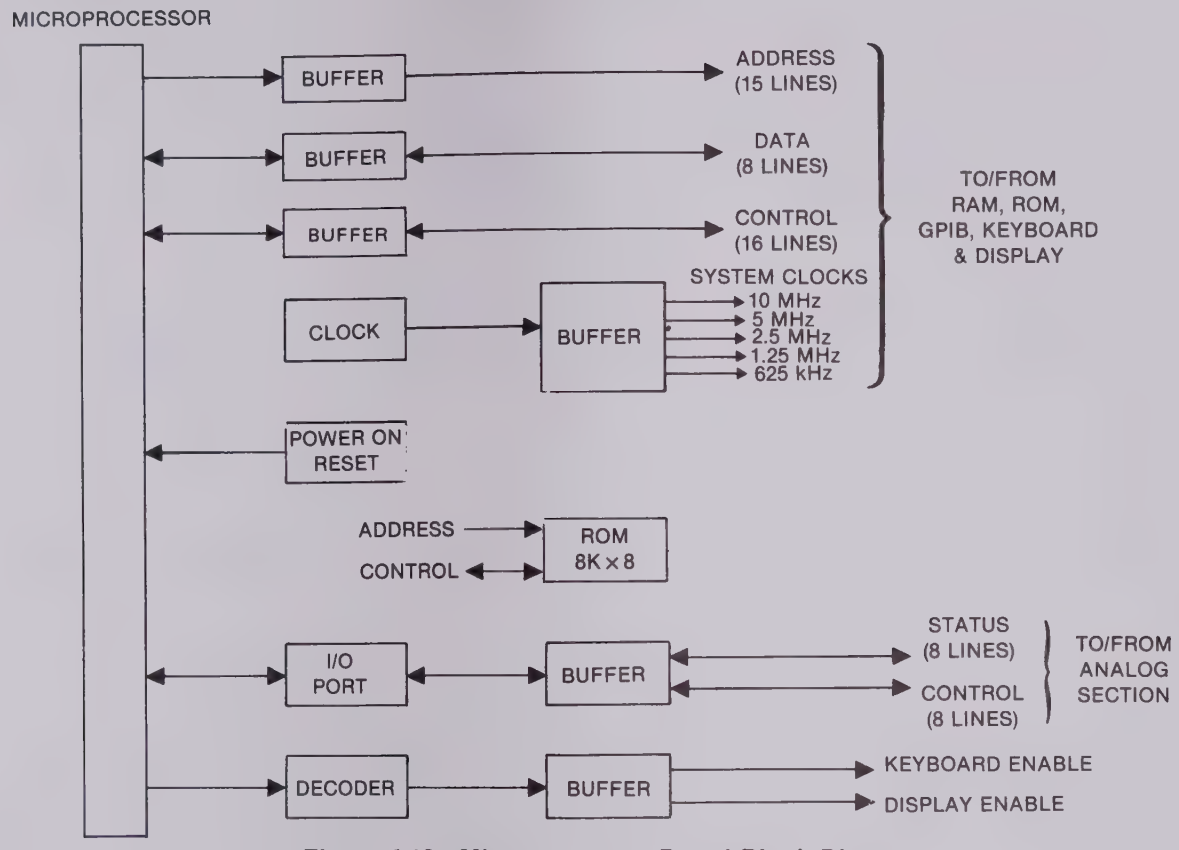


Figure 4-19. Microprocessor Board Block Diagram

shows the basic blocks of the microprocessor. Address lines are buffered to the mother board. Eight bidirectional data lines are received and driven to the mother board. Control signals necessary to describe the transaction are buffered to the mother board. Ten megahertz clock pulses are generated and buffered to the mother board. Clocks are available down to 625 kHz for other processor cards. All these signals are common to the processor section, but are not carried to the analog sections of the instrument (function generator and synthesizer).

Integrated circuit memories on ROM support the basic program in the 172B.

An I/O port generates eight control lines sent to the analog section of the instrument. These control lines are used to provide the microprocessor a facility to trigger the instrument or provide other control functions as options.

Eight status lines are sent to the microprocessor to indicate that a synthesizer has been installed and if the synthesizer is phase locked.

4.9.2 Memory RAM Board

The memory RAM board (see figure 4-20) contains 4096 eight bit bytes of volatile storage composed of eight 4K × 1 dynamic RAM chips. Refresh logic is located on this board with the logic necessary to arbitrate between a refresh cycle and a microprocessor cycle. In addition, the RAM board contains a 16 byte read/write scratch pad memory that transmits all data to the analog section of the instrument in 5 μs.

The RAM address is set to 6000_{16} through $6FFF_{16}$. A read or write is initiated by the microprocessor by using an operation request within the address space 6000_{16} to $6FFF_{16}$. If a refresh cycle is not in progress, data are accepted or presented depending upon the transaction requested on the data bus and an operation acknowledge is asserted. Data are latched until accepted and the microprocessor has removed the operation request signal.

The RAM stores up to 240 complete instrument settings. The contents of the RAM are lost whenever power is shut down.

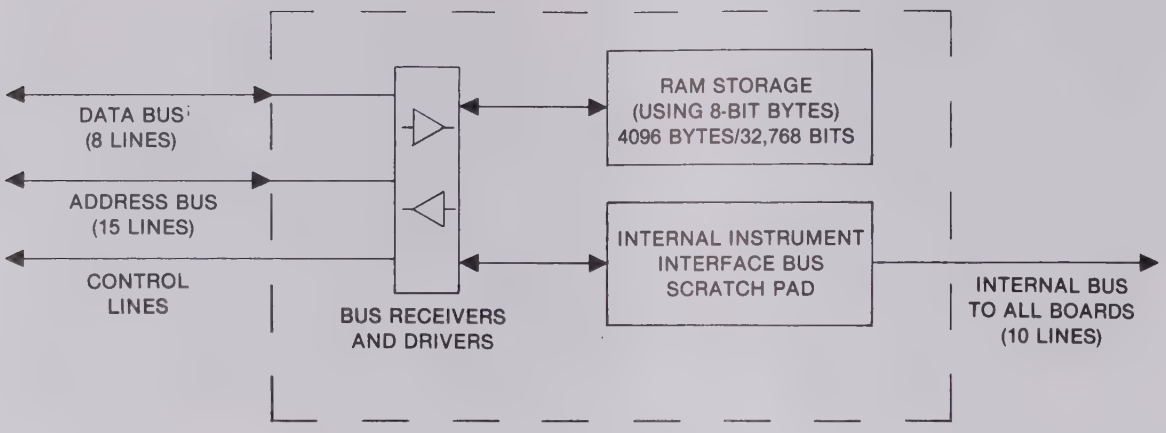


Figure 4-20. RAM (Random Access Memory) Writable and Readable for Data Storage Block Diagram

The RAM card includes a 16 byte scratch pad memory containing the data to be sent to the analog sections of the instrument. Data are transferred at a rate of four BCD characters per microsecond along with four address lines to all analog modules. Each line is terminated on the mother board. Scratch pad locations are accessed by the microprocessor and filled with properly formulated data for each analog module. Table 4-1 indicates the location of the data transferred to analog modules. All data are coded in four bit BCD digits. There is frequency and amplitude overranging in the most significant digits, as indicated by 12_{10} and 14_{10}, respectively, in table 4-1.

These values may differ from those transmitted to the instrument from a controller. The microprocessor selects its method of getting the output, then fills the scratch pad with properly formatted data. Data are sent to analog modules only when an execute command or GET is received.

4.9.3 Data Format

The internal data format for control parameters is as follows.

1. Offset — Three digits of offset are transferred with an allowable value in the range of 0 ± 7.49. The amplitude range digit will determine the actual voltage range selected.

2. Frequency — Five digits of frequency plus one range digit and sign are transferred within 2 μs. The function generator receives three digits from scratch pad locations 4 and 5 and one range digit plus sign bit. The synthesizer receives all five digits, but does not store the range digit. The most significant digit may be overranged to 12 on the 10^8 range for a maximum frequency of 12.9999 MHz. The range digit is the power-of-ten multiplier required (the decimal point follows the most significant digit).

3. Amplitude — Three digits of amplitude are transferred to the attenuator module and one digit to the power amplifier attenuator. Sign bits for amplitude and range digits are also transferred.

   The MSD of amplitude may be overranged to a value of 14.99 by transferring a 14 in the most significant digit on the top range (10^0). Therefore, the amplitude value can extend from 0 to 999 and be overranged to 14.99. All digits are BCD coded, sign-magnitude fashion (3 digits). An asserted sign bit indicates a negative value. The value is not complemented if the sign bit is set.

4. Symmetry — A one digit value from 0 to 9 selects the symmetry required. Zero and five select 50%, while digits 1 through 9 select symmetries at 10% intervals.

Table 4-1. Scratch Pad Memory Format

Data Sending Sequence	Address				Sign Bit		Data Byte								
	Group		Byte												
	A3	A2	A1	A0	S	Description	D7	D6	D5	D4	Description	D3	D2	D1	D0	Description
0	OFFSET (00)	0	0	0	0 1	+ OFFSET − OFFSET	0 0	0 1	0 1	0 1	DC OFFSET MSD 0 - 7_{10}	0 1	0 0	0 0	0 1	DC OFFSET MD 0 - 9_{10}
1		0	0	1							NOT USED	0 1	0 0	0 0	0 1	DC OFFSET LSD 0 - 9_{10}
2		0	0	1	0						NOT USED					NOT USED
3		0	0	1	1						NOT USED					NOT USED
4	FREQUENCY (01)	0	1	0	0		0 1	0 1	0 0	0 0	FREQUENCY MSD (5) 0 - 12_{10}	0 1	0 0	0 0	0 1	FREQUENCY DIGIT (4) 0 - 9_{10}
5		0	1	0	1	0 1	FREQ MULT + FREQ MULT −	0 1	0 0	0 0	0 1	FREQUENCY DIGIT (3) 0 - 9_{10}	0 0	0 1	0 1	0 0	FREQ MULT $10^{-4} \rightarrow 10^{0} \rightarrow 10^{+6}$
6		0	1	1	0		0 1	0 0	0 0	0 1	FREQUENCY DIGIT (2) 0 - 9_{10}	0 1	0 0	0 0	0 1	FREQUENCY DIGIT (1) 0 - 9_{10}
7		0	1	1	1						NOT USED					NOT USED
8	AMPLITUDE (10)	1	0	0	0	0 1	NORMAL INVERTED (OUTPUT)	0 1	0 1	0 1	0 0	AMPLITUDE MSD 0 - 14_{10}	0 1	0 0	0 0	0 1	AMPLITUDE MD 0 - 9
9		1	0	0	1	0	AMPL MULT + AMPL MULT −	0 1	0 0	0 0	0 1	AMPLITUDE LSD 0 - 9_{10}	0 0	0 0	0 1	0 1	AMPL MULT $10^{0} \rightarrow 10^{-3}$ 0 dB → − 60 dB
A		1	0	1	0						NOT USED					NOT USED
B		1	0	1	1						NOT USED					NOT USED
C	MODE (11)	1	1	0	0						**Function** SINE TRIANGLE SQUARE DC					**Mode** CONTINUOUS GATED TRIGGERED GATED HVRSN TRIG HVRSN SYNTHESIZE* EXT LOCK
												0 0 0 0 0 1 1	0 1 1 1 1 0 0	0 0 1 1 1 0 0	0 0 0 0 1 0 1	

Table 4-1. Scratch Pad Memory Format (Continued)

Data Sending Sequence	Address				Sign Bit		Data Byte									
	Group		Byte													
	A3	A2	A1	A0	S	Description	D7	D6	D5	D4	Description	D3	D2	D1	D0	Description
D	MISCELLANEOUS (11)	1	1	0	1						Symmetry					Load Output / Load
							0	0	0	0	50%					
							0	0	0	1	10%			0	0	OFF OUT
							0	0	1	0	20%			0	1	OFF IN
							0	0	1	1	30%			1	0	ON OUT
							0	1	0	0	40%			1	1	ON IN
							0	1	0	1	50%					
							0	1	1	0	60%					
							0	1	1	1	70%					
							1	0	0	0	80%					
							1	0	0	1	90%					
E		1	1	1	0						NOT USED					NOT USED
F		1	1	1	1						NOT USED					NOT USED

*Option

5. Function — A one digit value selects the requested function. These values differ from those used to command the instrument from the keyboard or the GPIB.

6. Mode — A one digit value selects one of seven modes. These values differ from those used to command the instrument from the keyboard or the GPIB.

7. Load — A one digit value selects the load and enables the output. These values also differ from those used to command the instrument from the keyboard or GPIB.

4.10 GPIB/MICROPROCESSOR INTERFACE

The GPIB/microprocessor interface allows the instrument to be remotely programmed by a minicomputer, calculator, etc., via the General Purpose Interface Bus (GPIB). The GPIB interface is an implementation of IEEE Standard 488-1975. It supports the following 488-1975 defined interface functions: Source Handshake (SH1), Acccepter Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL1), Device Clear (DC1) and Device Trigger (DT1). This bus transfers messages in bit parallel and byte serial fashion. The bus has 16 signal lines, and they are:

8 Data lines (DIO1 through DIO8)

5 Control lines (ATN, IFC, SRQ, EOI and REN)

3 Handshake lines (NRFD, NDAC and DAV)

These lines are defined in paragraph 3.6, as is operation with the GPIB.

The GPIB/microprocessor interface does the following three functions:

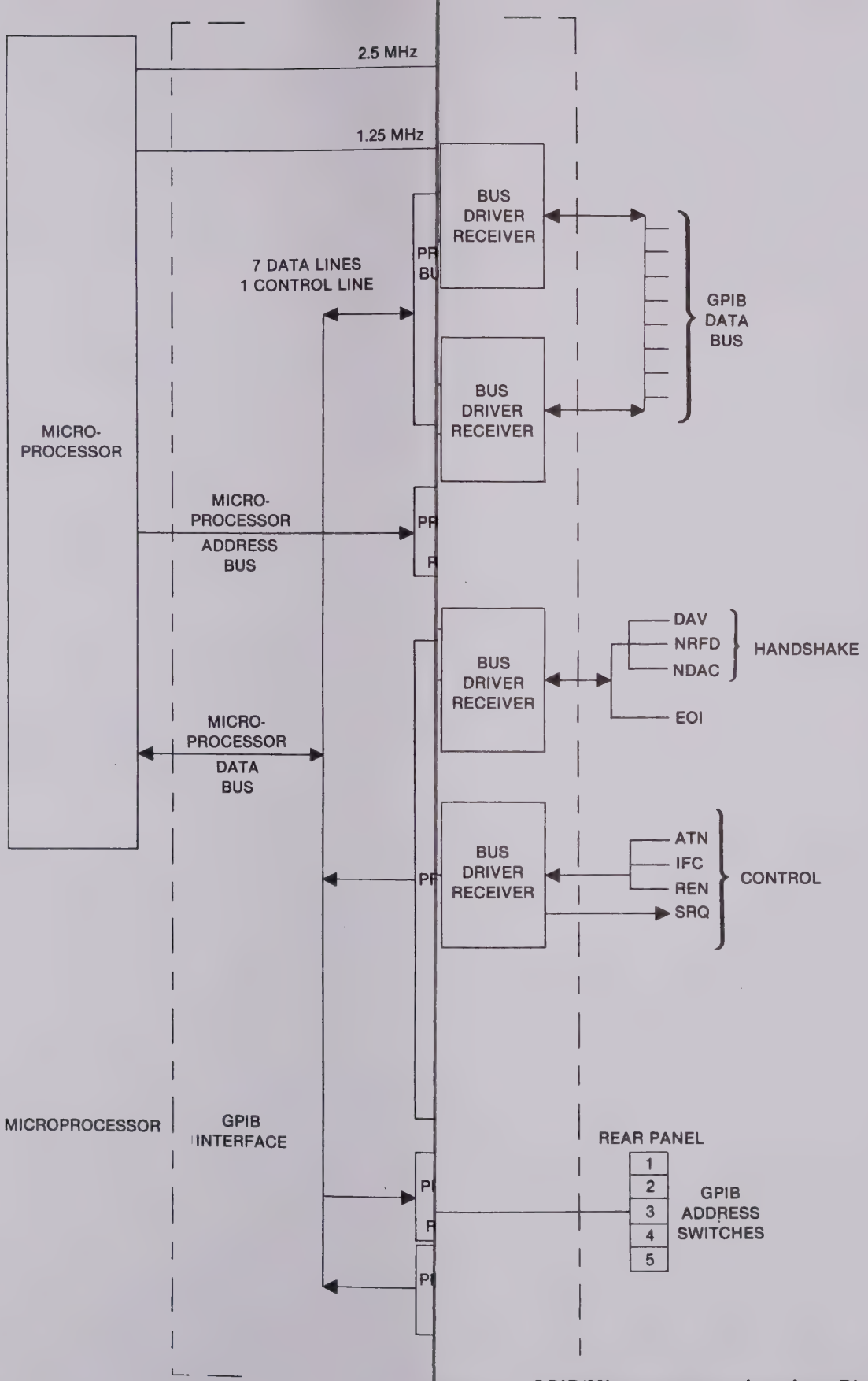
1. Detects the My Listen Address (MLA) and My Talk Address (MTA).

2. Does the proper listen handshake when either attention (ATN) is true, or the listen latch is set, and transfers messages when the talk latch is set.

3. Provides isolation through optical couplers.

In order to reduce the number of opto-isolators, the messages are transferred in bit serial fashion through two Universal Asynchronous Receiver/Transmitters (UART). (See figure 4-21.) All 16 GPIB lines are buffered and terminated through bus transceivers. The UART and status outputs are connected to the microprocessor data line via tri-state buffers.

The operation of the UART is fairly simple. Each UART consists of two independent sections called receiver



ure 4-21. GPIB/Microprocessor Interface Block Diagram

and transmitter, and both of them may operate simultaneously. The UARTs are primarily used to convert parallel information into serial and serial information into parallel. The receiver receives its information in serial and converts it into an 8 bit parallel byte, whereas the transmitter converts an 8 bit parallel byte into bit serial output. The transfer rate of the serial output is determined by the clock frequency of the UART. Here the UART clock frequency is set at 1.25 MHz.

The interface completely insulates the microprocessor from GPIB and hence the microprocessor is relieved from the GPIB transactions. The microprocessor constantly monitors the status outputs from the interface and takes actions according to that. There are six status bits tied to the microprocessor data bus: Data Ready, GPIB Busy, End, Remote, Talk and Listen.

4.10.1 Data Ready

The Data Ready bit informs the microprocessor that the UART has received valid data from the GPIB. Only when this bit is true will the microprocessor read the byte from the UART.

4.10.2 GPIB Busy

The GPIB Busy bit is used during the talk mode to find out whether GPIB has accepted the data byte sent through the UART. Any time the microprocessor wants to send a byte via GPIB, first it checks that the Talk status bit is true and then it checks that GPIB Busy status bit is false. If the GPIB Busy status is false, then the microprocessor will load a byte into the UART and cause the GPIB Busy signal to go high (true). This prevents the microprocessor from loading any more bytes into the UART. The byte loaded into the UART is transmitted serially across the optocoupler to the GPIB side of the UART. When all the 8 bits of the byte are present, the data valid (DAV) line is set low. When the listener on the GPIB senses the DAV line is low, he accepts the byte by raising the data accepted (NDAC) signal high. The NDAC signal is received and causes the GPIB Busy signal to go low (false). Once the GPIB Busy signal goes low, the microprocessor can transmit another byte in the same manner.

4.10.3 End

The End bit is monitored by the microprocessor any time it reads a byte from the UART. If this bit is true, then the microprocessor assumes that it has received the last byte of the message sequence and treats it as a terminating character.

4.10.4 Remote

The Remote bit indicates to the microprocessor whether the 172B is in remote control or local control.

4.10.5 Talk

The Talk bit will be set any time the 172B receives its assigned talk address. When the microprocessor senses this bit as true, it sends the appropriate talk message.

4.10.6 Listen

The Listen bit will be sent any time the 172B receives its assigned listen address. When the microprocessor senses this bit as true, it prepares to receive the data bytes through the UART.

4.10.7 Service Request

Service Request (SRQ) is a bit sent by the microprocessor to the GPIB when it wants to talk. The controller will eventually cause a talk status bit to be generated and allow the microprocessor to place a talk byte on the interface.

4.11 POWER SUPPLY

The power supply consists of the Pass Transistor board, the Power Supply Regulator board and the rear panel mounted transformer. The pass transistor board contains power transistors plus three IC regulators for the power supplies, while rectifier, regulator, reference and sensing circuits are on the regulator board.

The +24 volt voltage reference is a zener diode, and the −24 volt supply, in turn, uses the +24 volts as reference. (See figure 4-22.) The regulator sections are current limiting stages, which limit the power supply current under supply overload conditions. The + and −15 volt supplies (not shown in figure 4-22) operate in the same manner.

The +12, −5 and isolated +5 volt supplies (not shown in figure 4-22) use IC regulators located on the pass transistor board. The ground reference for the isolated +5 volt supply is isolated from common ground. System ground, isolated +5 volt ground and chassis ground are isolated from one another.

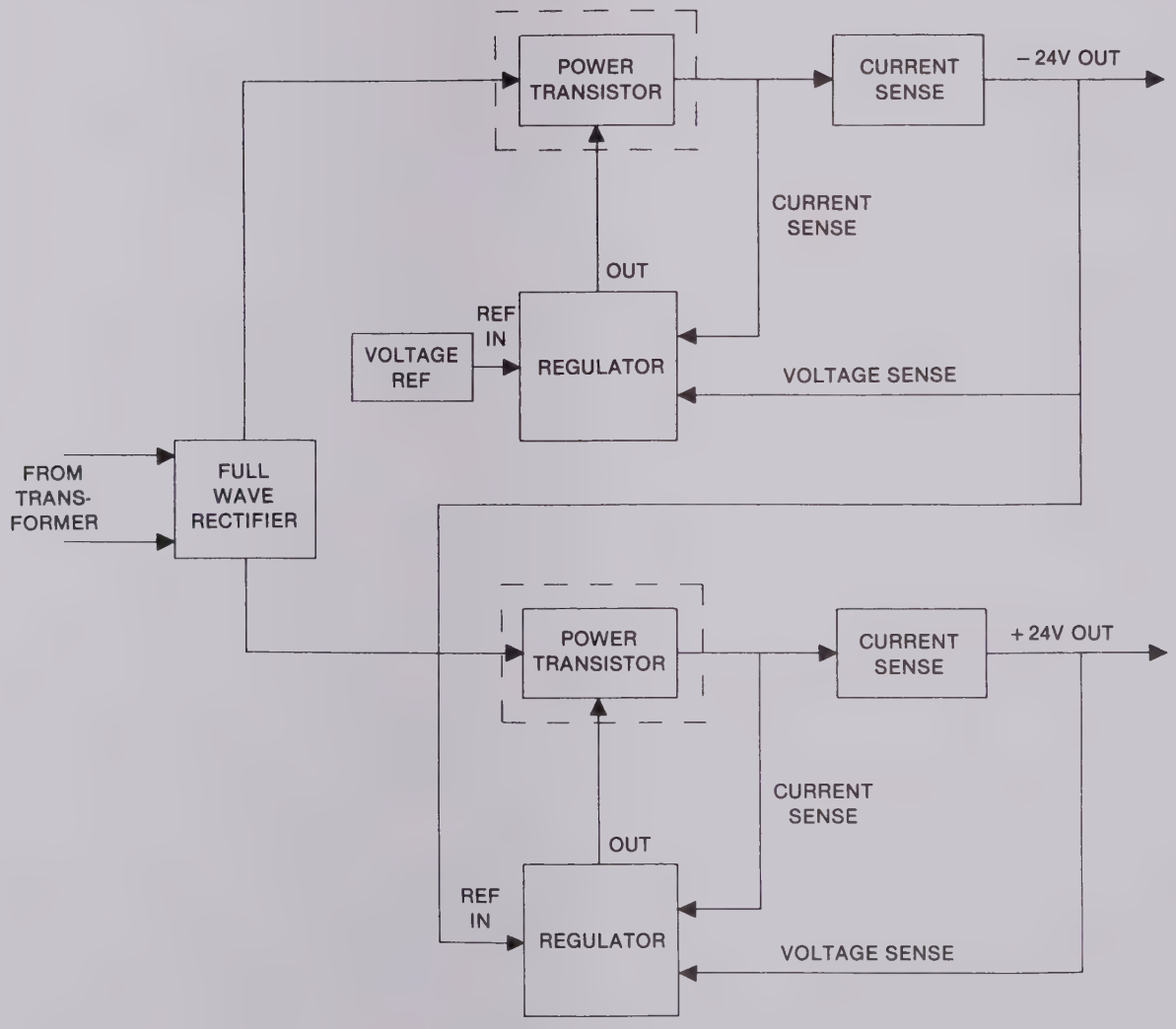


Figure 4-22. Power Supply Block Diagram

SECTION 5
TROUBLESHOOTING

5.1 INTRODUCTION

Faults may be isolated to circuit board, power supply or front panel. Familiarize yourself with the 172B by reviewing the operating procedures in this manual as well as the circuit descriptions. Successful fault isolation depends upon a thorough knowledge of the correct instrument operation.

Major groups of the various assemblies are shown in table 5-1. Fault isolation is discussed in the following paragraphs in terms of these groups. The locations of boards and assemblies called out in table 5-1 are shown in figure 4-1.

Table 5-1. Assembly Guide

Board Ejector Color	Assembly	Group
Black Black NA	Pass Transistor/Regulator Power Supply Regulator Rear Panel (Transformer, Capacitors, etc.)	Power Supply
Yellow Green Blue Gray Violet	VCG and Symmetry Triangle Generator Function/Preamp Power Amplifier/DC Offset Three Digit Attenuator	Function Generator (function generator calibration usually required when any function generator board is replaced)
Orange Red Brown	Digit 1/Mixer Digits 2 and 3 Digits 4 and 5/Reference	Synthesizer (Option 002)
White White	Microprocessor Memory RAM	Microprocessor
White NA	GPIB Interface GPIB Decoder	GPIB Interface
NA	Front Panel	Front Panel (Option 001)

5.2 POWER SUPPLY

In case the generator is malfunctioning, power supply voltage is always the first thing to be checked. Test points for all power supplies are on top edge of the power supply and regulator board. Table 5-2 shows the supply distribution to each PC board.

If the power supply voltage is found to be lower than normal, it indicates there is an overloaded or short circuit condition in the system. Turn off the generator immediately to avoid further damage. Remove all PC boards that use the overloaded supply. Use an ohmmeter to find the board having a short circuit condition by measuring the impedance between the ground and the supply line. If this is not successful, do the following. (This procedure is not recommended for the +5V supply.)

1. Monitor the supply voltage with a voltmeter at the Power Supply Regulator board.
2. From table 5-2, locate all the PC boards related to the overloaded supply.
3. Remove one of the boards and turn on the generator just long enough to make a voltage reading from the voltmeter.
4. If the supply voltage was back to normal, the removed board was the defective board.
5. If supply voltage is not back to normal after all the PC boards have been tested, possibly the regulator board itself is defective.

5.3 FUNCTION GENERATOR

If the generator is malfunctioning, first check the power supply voltages (refer to paragraph 5.2). Because some problems are due to the system being out of calibration, calibrate the function generator before troubleshooting (refer to paragraph 6.3). Troubleshoot using table 5-3.

Table 5-2. Power Distribution

Board Ejector Color	Assembly	Power at Assembly Pin Number												
		+5	+, −5 +, −12 COM	−5	+5 ISO	GND ISO	+12	−12	+15	+, −15 +, −24 −250 COM	−15	+24	−24	−250
Yellow	VCG and Symmetry	19,20	22-24						33,34	26-28	30,31	43	41	
Green	Triangle Generator	19,20	22-24						33,34	26-28	30,31			
Blue	Function/Preamp	19,20	22-24						33,34	26-28	30,31			
Gray	Power Amplifier/ DC Offset	19,20	22-24						33,34	26-28	30,31	39,40	36,37	
Violet	Three Digit Attenuator	19,20	22-24											
Orange	Digit 1/Mixer	19,20	22-24	50					33,34	26-28	30,31			
Red	Digits 2 and 3	19,20	22-24	50					33,34	26-28	30,31			
Brown	Digits 4 and 5/ Reference	19,20	22-24	50					33,34	26-28	30,31			
White	Microprocessor	49-52	1,2,99, 100											
White	Memory RAM	49-52	1,2,99, 100	53			3							
White	GPIB Interface	49-52	1,2,99, 100	63,78	62,77									
NA	GPIB Decoder				P17-20	P17-19								
NA	Front Panel	J1-23 J2-1,2	J1-21 J2-3,4					J1-7 J2-24						J1-26

Table 5-3. Function Generator Troubleshooting

NOTE: This information is for frequency problems apparent while the generator is in open loop, continuous mode.

Symptom	Further Observation	Probable Cause	Cure
1. Frequency accuracy out of spec. Problem has to do with the three digit setting.	1. Problem always happens at the same setting(s), between 1.00 and 9.99 of every frequency decade.	1. Frequency D/A converter. 2. Frequency data latch. 3. Internal bus.	Replace VCG board.
	2. All frequencies too high or too low. Waveform time symmetry normal.	1. VCG gain control. 2. Triangle peak voltage too high or too low.	Replace VCG board or Triangle Generator board.
	3. Waveform time symmetry also out of spec.	Current generator.	Replace VCG board.
	4. Problem happens only at 1 to 13 MHz, or 100 kHz to 1 MHz. Also refer to Symptom 5.	Frequency compensation components.	Replace Triangle Generator board.
	5. Triangle waveform also distorted.	1. Frequency range switch. 2. Component connected to the triangle amplifier input.	Replace Triangle Generator board.

Table 5-3. Function Generator Troubleshooting (Continued)

NOTE: This information is for frequency problems apparent while the generator is in open loop, continuous mode.

Symptom	Further Observation	Probable Cause	Cure
2. Frequency accuracy out of spec. Problem has to do with the range multiplier.	1. Out of spec at one particular frequency decade, but greater than 0.999 Hz.	1. Frequency range switches or capacitors. 2. Frequency range data latch or decoder.	Replace Triangle Generator board.
	2. Less than 0.999 Hz.	1. Capacitance multiplier. 2. Frequency range data latch or decoder.	Replace Triangle Generator board.
3. Time symmetry out of spec.	1. Triangle waveform also nonlinear.	1. Frequency range switches. 2. Component connected to the triangle amplifier input.	Replace Triangle Generator board.
	2. Triangle waveform linear.	1. Current generator. 2. Current mirror circuit.	Replace Triangle Generator board.
	3. Time symmetry problem only at frequency 0.999 Hz or less.	Capacitance multiplier circuit.	Replace Triangle Generator board.
4. Low frequency (<100 kHz) sine distortion out of spec.	1. Time symmetry also out of spec.	Refer to Symptom 3 for time symmetry problem.	Replace Triangle Generator board.
	2. Nonlinear triangle waveform.	Refer to Symptom 1(5).	Replace Triangle Generator board.
	3. Triangle waveform appears to be good.	Sine converter circuit.	Replace Function/ Preamp board.
	4. All waveforms are badly distorted.	Preamp or power amplifier.	Replace Function/ Preamp board or Power Ampl/Offset board.
5. High frequency (>100 kHz) sine distortion out of spec.	1. Frequency accuracy out of spec at frequency >1 MHz.	1. Current generator is saturated. 2. Current mirror circuit is saturated. 3. Refer to Symptom 1(4).	Replace VCG board or Triangle Generator board.
	2. Square wave has excess overshoot or slow rise time.	Preamp or power amplifier.	Replace Function/ Preamp board or Power Ampl/Offset board.
	3. Square wave ok, but badly distorted triangle.	Triangle amplifier No. 1 or No. 2.	Replace Triangle Generator board.
	4. Otherwise.	Sine converter.	Replace Function/ Preamp board.

Table 5-3. Function Generator Troubleshooting (Continued)

NOTE: This information is for frequency problems apparent while the generator is in open loop, continuous mode.

Symptom	Further Observation	Probable Cause	Cure
6. Amplitude accuracy out of spec at 1 kHz.	1. All waveform amplitudes out of spec between 1V p-p and 15V p-p.	1. Three digit attenuator. 2. Internal bus.	Replace Attenuator board.
	2. Ratio is not correct when amplitude is ranging from 9.99, 0.999, 0.0999 to 0.00999V p-p.	1. Output attenuator. 2. Attenuator control logic. 3. Internal bus.	Replace Power Ampl/ Offset board.
	3. Inverting output ("−" amplitude) ok, but not normal output ("+" amplitude).	1. Noninverting amplifier. 2. Relay.	Replace Function/ Preamp board.
	4. Square wave amplitude out of spec.	Square wave shaper circuit.	Replace Function/ Preamp board.
	5. Triangle wave amplitude out of spec.	Gain control resistors.	Replace Function/ Preamp board.
	6. Excess amplitude roll off at high frequency.	1. Frequency compensation components. 2. Frequency compensation components in power amplifier.	Replace Function/ Preamp board. Replace Power Ampl/ Offset board.
7. DC offset problem.		1. DC offset circuit. 2. Offset control logic. 3. Internal bus.	Replace Power Ampl/ Offset board.
8. Trigger and gate problem.		Trigger logic and trigger amplifier.	Replace Triangle Generator board.
9. No waveform output at 50Ω OUT.	1. Voltage at 50Ω OUT is saturated to maximum positive or negative. SYNC OUT is normal.	1. Power amplifier. 2. Function/preamp.	Replace Power Ampl/ Offset board. Replace Function/ Preamp board.
	2. SYNC OUT is normal and dc voltage at 50Ω OUT is normal when dc voltage is selected.	Waveform switching relay and control logic.	Replace Function/ Preamp board.
	3. No SYNC OUT when continuous mode is selected.	1. Triangle generator loop. 2. Current mirror circuit. 3. Current generator.	Replace Triangle Generator board. Replace VCG board.
	4. Generator runs if diode CR15 in Hysteresis Switch subassy of Triangle Generator board is removed.	1. Trigger circuit. 2. GEN MODE control logic.	Replace Triangle Generator board.
10. Output waveform is not the waveform programmed.	No other programming error.	1. Function selecting relay. 2. Function control logic. 3. Internal bus.	Replace Function/ Preamp board.
11. Generator frequency does not lock to external frequency.	1. Phase not locked at all frequencies.	1. Generator frequency is not within ±2% of external frequency. 2. Phase detector or filter. 3. Input circuit.	Change the generator frequency. Replace VCG board.
	2. No phase lock at a frequency range.	Loop filter selection circuit.	Replace VCG board.

5.4 INTERNAL DATA BUS

All the internal programming data sent to the function generator and the frequency synthesizer sections are sent in multiplex fashion through the 14 internal bus lines. It takes only one defective bus receiver, 74LS139 or 74LS175, to hang up an entire line. A defective receiver can cause incorrect generator responses everywhere.

When the bus is not sending data, no EXECUTE command, the voltage at each bus is biased to approximately +3 volts. If the bus voltage is greater than +4 volts, or less than +2 volts, there is a defective bus receiver or driver on the line. The defective component can be located by removing one board at a time. The bus voltage will be back to normal when the defective board is removed. Table 5-4 gives the bus location.

Table 5-4. Internal Data Bus Location

Description	Bus Line	Pin No.*
Strobe	STRB	1
	A3	2
Data	A2	3
Group	A1	4
	A0	5
Sign	S	6
	D7	7
	D6	8
	D5	9
Data	D4	10
Byte	D3	11
	D2	12
	D1	13
	D0	14

NOTE

Table 4-2 describes the data content of each line on the internal data bus.

*PC-to-Mother board connector (Function Generator or Synthesizer boards).

5.5 SYNTHESIZER

When the 172B output frequency is incorrect in the synthesizer mode, the problem may be on one of the three synthesizer boards, or, it may be in the function generator section. The following checks in table 5-5 can be made external to the 172B with a frequency counter.

NOTE

Tests in the synthesizer mode are done on the 1 to 13 MHz range for two reasons. The natural output of the synthesizer is 1 to 13 MHz, so there is less chance of confusion; and the frequency counter will give high resolution readings with minimum gate time on this range.

Table 5-5. Synthesizer Troubleshooting

Symptom	Discussion
1. The function generator output frequency is correct on the 1 to 12.9999 MHz range, but is not correct on one or more lower ranges.	1. This indicates the synthesizer subassembly is functioning properly, and the problem is on the VCG board where the main function generator is phase locked to the synthesizer output. 2. When a particular range and all lower ranges do not work, and all higher ranges do work, the problem is in the decade digital divider string on the VCG board.
2. The output frequency is wrong on the 1 to 12.9999 MHz range, but one or more of the lower ranges works.	Check the open loop frequency (continuous mode, B0). If this frequency is greater than 4% from the programmed frequency, the function generator frequency may be outside the capture range of the function generator phase lock loop (PPL). (Refer to paragraph 5.3.)
3. There is no change in frequency switching between continuous (B0) and synthesized (B3) modes.	The VCG board is not receiving the digital command to switch into the synthesized mode. Check the front panel to make sure the display is not indicating a programming error. If there is no programming error, refer to Internal Data Bus, paragraph 5.4. Frequency must be greater than 10 Hz.
4. The 172B does not operate properly in synthesized mode, but does in external phase lock (B6) mode (with the proper external signal provided).	The main generator phase lock circuitry is operating properly and the problem is likely to be in the synthesizer section. Refer to Symptom 6. A good frequency source for the external phase lock check is the 10 MHz reference output available on the rear panel of the 172B. A different frequency such as 1 MHz may be available from the frequency counter used for testing.
5. The synthesized frequency is off by a small, constant percentage error at all frequencies.	The error is in the synthesizer time base, which is an adjustment located on the Digits 4 and 5/Reference PC board; adjust or replace the board.
6. There is a failure within the synthesizer.	1. An indication of the specific failure location can be obtained by a careful study of the actual output frequencies for a range of input frequencies. For example: Programmed frequencies from 1.0000 MHz to 1.0067 MHz work properly. Programmed frequencies from 1.0068 MHz to 1.0099 MHz give an output frequency of 1.0067. This pattern then repeats: 1.0100 thru 1.0167 work properly and 1.0168 thru 1.0199 give an output of 1.0167 MHz. This pattern also repeats at any other frequency: the first three digits work properly and the fourth and fifth digit work properly when programmed between 00 and 67. Armed with these data, and a knowledge of the synthesizer structure (refer to the synthesizer block diagrams in Section 4), you may deduce the problem lines within the digits 4 and 5 PLL located on the Digits 4 and 5/Reference PC board, or the translation loop located on the Digits 2 and 3 Translation Loop PC board. With these particular symptoms, it is likely the Voltage Controlled Oscillator (VCO) frequency has shifted in the translation loop or digits 4 and 5 loop, and can be corrected with a simple calibration adjustment. Determining which of these two possible loops are bad requires going inside the 172B and measuring the actual output of digits 4 and 5. If spare boards are available, substitution will reveal which of the two is defective faster than making on board measurements. 2. Another example: All programmed frequencies from 1.0000 thru 1.0099 MHz measure 1.0154 MHz; all programmed frequencies from 1.0100 thru 1.0199 measure 1.0254 MHz; all programmed frequencies from 1.0200 thru 1.0299 MHz measure 1.0354 MHz, etc. Again, the indications are that the digit 2, 3 loop and all following stages are operating correctly because the synthesizer follows each 10 kHz change in programmed frequency even though the output frequency is not correct. The digit 4, 5 loop or the translation loop is functioning incorrectly and outputting a single frequency instead of following the programming changes. Again with these symptoms, one of the two loops may have a defective component or the oscillator natural frequency may have shifted more than the loop can correct for, and repair consists of a simple calibration adjustment. Refer to the synthesizer calibration procedure.

5.6 MICROPROCESSOR

When microprocessor problems are suspected, always check the +5, −5 and +12V power supplies (refer to paragraph 5.2). If all voltages are present, use table 5-6 to troubleshoot. Replace board assemblies one at a time, until the problem is eliminated.

5.7 GPIB INTERFACE

Because the 172B has more than one programming channel (GPIB and front panel), it is relatively easy to isolate interface problems. (Refer to table 5-7.)

5.8 FRONT PANEL

The front panel assembly contains circuitry for two distinct functions; display and keyboard, both communicating with the microprocessor through the data and address busses. Because of the intimate relationship of the front panel and microprocessor, it can be difficult to isolate a problem to a particular area. (Refer to table 5-8 for troubleshooting hints.)

Table 5-6. Microprocessor Troubleshooting

Symptom	Possible Cure
1. 172B will not power up.	1. Replace RAM board. 2. Replace Microprocessor board.
2. 172B powers up, but gives ERROR when key is pressed.	1. Replace RAM board. 2. Replace Microprocessor board.
3. 172B powers up with ERROR in left margin.	1. Replace Microprocessor board. 2. Replace RAM board.
4. 172B powers up and reads different GPIB address other than the setting.	1. Check the isolated +5V (refer to paragraph 5.2). 2. Replace GPIB Interface board.
5. 172B will not talk or listen on GPIB.	1. Correct the listen address setting on rear panel. 2. Check the isolated +5V (refer to paragraph 5.2). 3. Replace GPIB Interface board.
6. While running, 172B resets itself and displays "WAVETEK MODEL 172B".	1. Replace Microprocessor board. 2. Replace RAM board.

Table 5-7. GPIB Interface Troubleshooting

Symptom	Discussion
1. When addressed as a listener or talker, the 172B does not display an L or T on the right-hand corner of the display.	Find the GPIB listen and talk addresses by pushing the ADR key. They will be displayed. Program the controller to send the listen address. (The HP 9825 controller message is wrt 7xx, where xx is the 172B address.) L, or RL, should appear on the right-hand corner of the display; if not, the malfunction is in the GPIB Interface board. The talk address problem is similarly dealt with.
2. Displayed parameter values differ from GPIB programmed values.	Use the CMD RCL key to display the programming received by the post-interface circuits. If this differs from GPIB programmed values, duplicate the programming by using the front panel controls. Correct display isolates the malfunction to the GPIB Interface board.

Table 5-8. Front Panel Troubleshooting

CAUTION: There is high voltage (−250 volts) present in the front panel.

Symptom	Discussion
1. When power is first turned on, the front panel readout displays "SELF TEST". After a short delay, the microprocessor commands the front panel to display "WAVETEK 172B". The message is not displayed.	If this message never appears, the problem can be on any of the digital boards. Most likely it is not a front panel problem. While a front panel failure could cause the front panel not to accept data, it is much more likely the microprocessor never reached the portion of the operating program that causes the initial display. Replace the Microprocessor and Memory RAM boards one at a time. Test the 172B with each replacement.
2. After the turn-on delay, the initial random characters are replaced by another meaningless display.	The microprocessor is reaching the front panel. Examine this message carefully for clues as to the possible problem; for example, "V@VDTDJ062B" instead of "WAVETEK 172B" would indicate the "1" bit of the data word was hung in a false condition. This could be occurring in the front panel bus receivers, memory or in the display component itself. Another type of failure mode might be "WAWATETE1717" indicating a hung "2" bit on the address lines driving the memory IC. In any case, the malfunction is most likely in the front panel.
3. The display is missing portions of characters or characters are jittering in position.	The problem is most likely the display component, although the −250V regulator could be causing the flicker. Replace the front panel.
4. The keyboard "beeps" normally when a key is depressed, but the processor ignores it (no response on the display).	The problem may be in the front panel or in the microprocessor. Command the 172B via the GPIB and check for proper operation. If the 172B cannot be commanded by any means, the problem is most likely not in the front panel. A front panel address or data bus driver or receiver could fail in a manner to permanently hang a bus line, preventing the microprocessor from operating properly. Unplug the front panel from the mother board (J20), with power off. Turn power back on and again try to command the 172B via GPIB. If the 172B runs properly, the problem is in the front panel.
5. The keyboard fails to "beep", but commands the 172B properly.	The problem is in the circuitry associated with the audio sounder. Replace the front panel.
6. The keyboard neither beeps or commands the 172B, but 172B works properly with the GPIB interface.	The problem is with the keyboard encoder, or the keyboard membrane switch itself. Replace the front panel.

SECTION 6
CALIBRATION

6.1 INTRODUCTION

The following four calibration procedures may be used to totally align the 172B periodically, or they may be used individually to calibrate the functional group to which they apply. Individual procedures would be used in the case of a circuit board replacement or for out-of-spec operation of a particular functional group.

The completion of these calibration procedures returns the instrument to correct calibration. All limits and tolerances given in these procedures are calibration guides and should not be interpreted as instrument specifications. Instrument specifications are given in section 1 of this manual.

The functional groups are shown in table 5-1 with a listing and location of individual assemblies within the groups. The microprocessor group and the GPIB group require no calibration. The calibration procedures included herein are:

Power Supply . . . . . paragraph 6.2
Function Generator . . . . . paragraph 6.3
Synthesizer . . . . . paragraph 6.4
Front Panel . . . . . paragraph 6.5

Periodic calibration of all groups is needed because of component aging, which depends on the instrument on-time and environment. Use three months as an initial calibration period. If possible, keep records of parameter values and increase the time between calibrations as the records indicate.

In any case, the power supplies should be verified or adjusted before attempting any other calibration procedure or fault isolation.

The air inlet for the instrument cooling fan contains a filtering screen that must be cleaned periodically. To clean, remove the screen retainer and screen (at the rear of the instrument). Vacuum or wash and dry the screen as necessary or annually.

6.2 POWER SUPPLY CALIBRATION/ VERIFICATION

Verify that line selector (refer to paragraph 2.2.1) matches the line voltage. Use a Dana 5900 DVM or equivalent to perform the procedures given in table 6-1.

6.3 FUNCTION GENERATOR CALIBRATION

Use the test equipment listed here, or equivalent, to perform the procedures given in table 6-2.

1. Frequency Counter: Dana Model 8110
2. DVM: Dana 5900
3. Distortion Analyzer: HP Model 334A
4. Oscilloscope: Tektronix Model 7904 with
   a. Dual Trace Amplifier 7A26
   b. Dual Time Base 7B92
   c. Differential Comparator 7A13
5. 50 Ohm 5W Termination: Tektronix 011-0099-00
6. Scope Probe: Tektronix P6101
7. Probe Tip BNC Adapter: Tektronix 013-0034-02

6.4 SYNTHESIZER CALIBRATION/VERIFICATION

Use the test equipment listed here, or equivalent, to perform the procedures given in table 6-3. If the verification portion of table 6-3 indicates that the synthesizer does not require calibration, only items No. 1 and No. 4 will be required as test equipment.

1. Frequency Counter: Dana 8110
2. RF Millivoltmeter: Boonton 92C
3. DVM: Dana 5900
4. 172B Extender Board: Wavetek

6.5 FRONT PANEL CALIBRATION

1. Repeatedly press any front panel switch to obtain an audio tone.
2. Adjust R15 on the front panel PC board for the greatest volume.

CAUTION

There are exposed high voltage points (250 volts) in the display section.

Table 6-1. Power Supply Calibration/Verification Procedures

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
1	+15V	DVM in dc mode	TP7 (gnd) TP6	Power ON (initial setup)	R24	+15.0 Vdc ±20 mV	All test points and adjustments are located on power supply regulator bd.
2	−15V		TP8			−15.0 Vdc ±100 mV	Verify.
3	+12V		TP10			+12.0 Vdc ±350 mV	
4	−5V		TP11			−5.0 Vdc ±100 mV	
5	+5V (iso)		TP14 (gnd) TP13			+5.0 Vdc ±200 mV	
6	+24V		TP3 (gnd) TP5		R10	+24.0 Vdc ±200 mV	
7	−24V		TP4			−24.0 Vdc ±200 mV	Verify.
8	+5V (logic)		TP15 (gnd) TP12		R58	+5.0 Vdc ±100 mV	

Table 6-2. Function Generator Calibration Procedures

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
1	Trigger Baseline	DVM in dc mode	TP1 (function/ preamp bd)	FREQ: 9.99E2 FUNC: 4 OUTP: 1 MODE: 1 AMPL: −10 EXEC	R54 (triangle gen bd)	0V ±10 mVdc	999 Hz, inverted, 10V p-p, dc, trig mode. Allow 1 hour warm-up.
2	Symmetry Zero		TP2 (triangle gen bd)		R124 (triangle gen bd)	0V ±1 mVdc	
3	Inverted Zero		TP3 (function/ preamp bd)		R53 (function/ preamp bd)	0V ±2 mVdc	
4	Standard Zero		TP2 (function/ preamp bd)		R79 (function/ preamp bd)		
5	Offset Inverted Zero		TP4 (pwr ampl/ offset bd)		R75 (pwr ampl/ offset bd)	0V ±5 mVdc	
6	Offset Standard Zero		TP2 (pwr ampl/ offset bd)		R72 (pwr ampl/ offset bd)		

Table 6-2. Function Generator Calibration Procedures (Continued)

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
7	Power Amplifier Zero		50Ω OUT (rear panel)		R53 (pwr ampl/ offset bd)	0V ±1 mVdc	
8	Positive Triangle Peak	Scope with comparator	TP1 (function/ preamp bd)	FUNC: 2 MODE: 0 EXEC	R79 (triangle gen bd)	+2V ±10 mVp	cont mode.
9	Negative Triangle Peak				R76 (triangle gen bd)	−2V ±10 mVp	
10	1000:1 Symmetry	2 channel scope with 50Ω load	50Ω OUT (rear panel)	OUTP: 0 FREQ: 1E4 EXEC FREQ: 0 EXEC R28 (VCG bd): ccw	R58, R75 (VCG bd)	5 ±0.5 ms on each ½ cycle (100 ±10 Hz) (use scope with 1 ms/div sweep)	, no internal load (load at scope). 10 kHz range, 0 Hz; R58 and R75 settings must be done in sequence.
11	Bottom Symmetry			FREQ: 1E2 EXEC	R33 (VCG bd)	Symmetry ±0.1% (10 μs)	
12	Top Symmetry			FREQ: 9.99E2 EXEC	R67 (VCG bd)	Symmetry ±0.1% (1 μs)	
13	High Frequency Symmetry			FREQ: 1E5 EXEC	R72 (VCG bd)	Symmetry ±0.3% (30 ms)	Repeat steps 11 - 13 until all settings are in tolerance.
14	Bottom Frequency	Counter		FREQ: 1E2 EXEC	R28 (VCG bd)	100 ±1 Hz	
15	Top Frequency			FREQ: 9.99E2 EXEC	R21 (VCG bd)	999 ±5 Hz	Repeat steps 14 and 15 until all settings are in tolerance.
16	Frequency		50Ω OUT (rear panel)	FREQ: 12.99E6 EXEC	C41 (triangle gen bd)	12.99 MHz ±50 kHz	Check over 1 - 12.99 range and distribute the error. Verify 1E6 (±5%) and 1E7 (±4%).
17				FREQ: 9.99E5 EXEC	R22 (VCG bd)	999 ±5 kHz	
18				FREQ: 9.99E4 EXEC	C44 (triangle gen bd)	99.9 kHz ±500 Hz	
19				FREQ: 9.99E3 EXEC	R20 (VCG bd)	9.99 kHz ±50 Hz	
20				FREQ: 9.99E1 EXEC	R18 (VCG bd)	0.01001s ±50 μs (50 μs)	
21				FREQ: 9.99 EXEC	R17 (VCG bd)	0.1001s ±0.5 ms (0.5 ms)	
22				FREQ: 9.99E-1 EXEC	R120 (triangle gen bd)	1.001s ±5 ms (5 ms)	

Table 6-2. Function Generator Calibration Procedures (Continued)

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
23	HF Aberrations	2 channel scope with 50Ω load		FREQ: 1E6 EXEC	C12 (pwr ampl/ offset bd)	Best	<5% overshoot
24	Sine	Scope with comparator & distortion analyzer; load removed		FREQ: 9.99E2 FUNC: 0 OUTP: 1 EXEC	R11 (function/ preamp bd)	+5V ±20 mVdc at positive peak	Internal load, 999 Hz output. Center R45 on pwr ampl/offset bd.
25					R9 (function/ preamp bd)	−5V ±20 mVdc at negative peak	
26					R107 (function/ preamp bd)	Symmetrical residue	Connect scope to distortion analyzer output.
27					R1 (function/ preamp bd)	Minimum distortion (0.15% typ)	After this step, repeat steps 24 thru 26 once.
28	Negative Sine Unity Gain	DVM in ac mode			R45 (pwr ampl/ offset bd)	3.535V ±3 mVrms	
29	Positive Sine Unity Gain			AMPL: 10 EXEC	R95 (function/ preamp bd)	3.535V ±3 mVrms	
30	Gain			FUNC: 1 EXEC	R5 (function/ preamp bd)	2.775V ±3 mVrms	With average responding DVM. Otherwise, use comparator to set peaks to ±5 Vp ±20 mV.
31	Positive peak	DVM in dc mode	50Ω OUT (rear panel)	FUNC: 2 FREQ: 0.1 EXEC	R36 (function/ preamp bd)	+5 Vp ±10 mV	Slow output, internal load.
32	Negative peak				R43 (function/ preamp bd)	−5 Vp ±10 mV	
33	+DC Offset Gain			FUNC: 4 OFST: +7.49 EXEC	R62 (pwr ampl/ offset bd)	+7.49V ±20 mVdc	+7.49 Vdc output, internal load.
34	−DC Offset Gain					−7.49V ±20 mVdc	Verify.
35	Haver Baseline			FUNC: 1 OFST: 0 AMPL: 10 MODE: 5 FREQ: 999 EXEC	R37 (triangle gen bd)	−5V ±50 mVdc	Gated havertriangle baseline output.

Table 6-3. Synthesizer Calibration/Verification

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
1	Time Base	Counter	REF OUT (rear panel)	Power ON (initial settings)	L2 (digits 4 & 5 bd)	10.00000 MHz ±50 Hz	Allow 1 hour warm-up.
2	Verify 12.9999E6		50Ω OUT (rear panel)	FREQ: 12.9999E6 FUNC: 2 AMPL: 10 OUTP: 1 MODE: 3 EXEC		12.99990 MHz ±65 Hz	Verify.
3	Verify 10.9999E6			FREQ: 10.9999E6 EXEC		10.99990 MHz ±55 Hz	
4	Verify 9.9999E6			FREQ: 9.9999E6 EXEC		9.99990 MHz ±50 Hz	
5	Verify 999 Hz			FREQ: 999 EXEC		999.000 Hz ±5 mHz	
6	Verify 10 Hz			FREQ: 10 EXEC		**10.00000 Hz ±500 μHz**	It is normal for this reading to show some cycle-to-cycle jitter.
	This completes the verification portion of this procedure. If negative results were obtained, complete the calibration procedure before attempting fault isolation.						
7	30 MHz Multiplier	RF milli-voltmeter	TP3 (digits 4 & 5 bd)	Power ON (initial settings)	L3 (digits 4 & 5 bd 30 MHz MULT)	Maximum reading	Place digits 4 & 5 bd on the extender bd. Remove shield. Connect probe gnd lead to board common as near TP3 as possible.
8	60 MHz Multiplier		TP4		L4 (digits 4 & 5 bd	Maximum reading	*Note: Turn instrument power OFF while removing or replacing boards.*
9	Digits 4 & 5 VCO	DVM	Junction CR1/C3	FREQ: 10.9999E6 EXEC	L1 (digits 4 & 5 bd 40 MHz VCO)	1.70 Vdc	Connect DVM ground to board common.
10	Translation Loop VCO		Terminal VC on 60.4 MHz Module		C1	1.30 Vdc	Replace digits 4 & 5 bd and place digits 2 & 3 bd on the extender bd (2 if possible). Connect DVM ground to 60.4 MHz module common. C1 is the trimmer capacitor protruding from the underside of the 60.4 MHz module.
11	Digits 2 & 3 VCO		Terminal VC on 40 MHz module (digits 2 & 3 bd)		L1	3.50 Vdc	Connect DVM gnd to 40 MHz module case. L1 is accessible thru a hole in top of the 40 MHz module.

Table 6-1. Power Supply Calibration/Verification Procedures (Continued)

Step	Check	Tester	Cal Points	Program	Adjust	Desired Results	Remarks
12	Digit 1 VCO		Pin VC on 35 MHz module A1 (digit 1/ mixer)	FREQ: 1.0000E6 EXEC		3.46 Vdc	Replace digits 2 & 3 bd and place digit 1/mixer on the extender bd. L1 is accessible thru a hole in top of the 35 MHz module.
13	Output Mixer	RF milli-meter	TP2	FREQ: 5.8500E6 EXEC	L7 (30 MHz BPF)	Maximum reading	
14			TP3		L11, L12 (input mixer)		
15			TP4		L13, L14 (34.5 MHz BPF)		After this step, reinstall digit 1/mixer board.

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, parts lists and schematics are in the arrangement shown below.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and the function performed.

The part numbers for printed circuit boards are etched on the boards just as the circuits are. When the boards are loaded with components the boards are considered **assemblies** and stamped with **assembly** numbers. These same numbers are found in the parts lists. Each printed circuit **assembly** has its own parts list; the parts list number is the **assembly** number. The printed circuit board will appear as a component in the parts list.

7.3 ADDENDA

Under Wavetek's product improvement program, the latest designs are incorporated into each instrument as quickly as development and testing permit. Because of the time needed to prepare manuals, it is not always possible to include the most recent changes. Whenever this occurs, addendum pages are prepared and inserted.

Drawing	Drawing No.
Chassis Assembly	0102-00-0726
Chassis Parts List	1101-00-0726
Front Panel Assembly	0102-00-0968
Front Panel Parts List	1101-00-0968
Front Panel Logic Schematic	0103-00-0938
Front Panel Logic Assembly	0101-00-0938
Front Panel Logic Parts List	1100-00-0938
Rear Panel Schematic	0104-00-0792
Rear Panel Assembly	0102-00-0792
Rear Panel Parts List	1101-00-0792
GPIB Decoder Schematic	0103-00-0554
GPIB Decoder Assembly	0101-00-0554
GPIB Decoder Parts List	1100-00-0554
Mother Board Assembly	0101-00-0717
Mother Board Parts List	1100-00-0717
Signal Routing on Mother Board	-----
Pass Transistor/Regulator Schematic	0103-00-0713
Pass Transistor/Regulator Assembly	0101-00-0713
Pass Transistor/Regulator Parts List	1100-00-0713
Power Supply Regulator Schematic	0103-00-0712
Power Supply Regulator Assembly	0101-00-0712
Power Supply Regulator Parts List	1100-00-0712

Drawing	Drawing No.
Memory RAM Schematic	0103-00-0708
Memory RAM Assembly	0101-00-0708
Memory RAM Parts List	1100-00-0708
Microprocessor Schematic	0103-00-0699
Microprocessor Assembly	0101-00-0699
Microprocessor Parts List	1100-00-0699
GPIB Interface Schematic	0103-00-0685
GPIB Interface Assembly	0101-00-0685
GPIB Interface Parts List	1100-00-0685
Power Amplifier/DC Offset Schematic	0103-00-0710
Power Amplifier/DC Offset Assembly	0101-00-0710
Power Amplifier/DC Offset Parts List	1100-00-0710
Power Amplifier Subassembly No. 1 Assembly	0101-00-0591
Power Amplifier Subassembly No. 1 Parts List	1208-00-0591
Power Amplifier Subassembly No. 2 Assembly	0101-00-0592
Power Amplifier Subassembly No. 2 Parts List	1208-00-0592
Power Amplifier Subassembly No. 3 Assembly	0101-00-0593
Power Amplifier Subassembly No. 3 Parts List	1208-00-0593

Drawing	Drawing No.
3 Digit Attenuator Schematic	0103-00-0715
3 Digit Attenuator Assembly	0101-00-0715
3 Digit Attenuator Parts List	1100-00-0715
Function/Preamp Schematic	0103-00-0707
Function/Preamp Assembly	0101-00-0707
Function/Preamp Parts List	1100-00-0707
Triangle Generator Schematic	0103-00-0714
Triangle Generator Assembly	0101-00-0714
Triangle Generator Parts List	1100-00-0714
Hysteresis Switch, Triangle Generator Assembly	0101-00-0558
Hysteresis Switch, Triangle Generator Parts List	1208-00-0558
Trigger, Triangle Generator Assembly	0101-00-0559
Trigger, Triangle Generator Parts List	1208-00-0559
Buffer Amplifier, Triangle Generator Assembly	0101-00-0560
Buffer Amplifier, Triangle Generator Parts List	1208-00-0560
VCG and Symmetry Schematic	0103-00-0711
VCG and Symmetry Assembly	0101-00-0711
VCG and Symmetry Parts List	1100-00-0711

Drawing	Drawing No.
Digit 1/Mixer Schematic	0103-00-0706
Digit 1/Mixer Assembly	0101-00-0706
Digit 1/Mixer Parts List	1100-00-0706
35/40 MHz VCO Module, Digit 1/Mixer Schematic	0104-00-0519
35/40 MHz VCO Module, Digit 1/Mixer Assembly	0102-00-0519
35/40 MHz VCO Module, Digit 1/Mixer Parts List	1206-00-0519
Digits 2 & 3 Schematic	0103-00-0704
Digits 2 & 3 Assembly	0101-00-0704
Digits 2 & 3 Parts List	1100-00-0704
60.4 MHz VCO Module, Digits 2 & 3 Schematic	0103-00-0520
60.4 MHz VCO Module, Digits 2 & 3 Assembly	0102-00-0520
60.4 MHz VCO Module, Digits 2 & 3 Parts List	1206-00-0520
Digits 4 & 5/Reference Schematic	0103-00-0705
Digits 4 & 5/Reference Assembly	0101-00-0705
Digits 4 & 5/Reference Parts List	1100-00-0705

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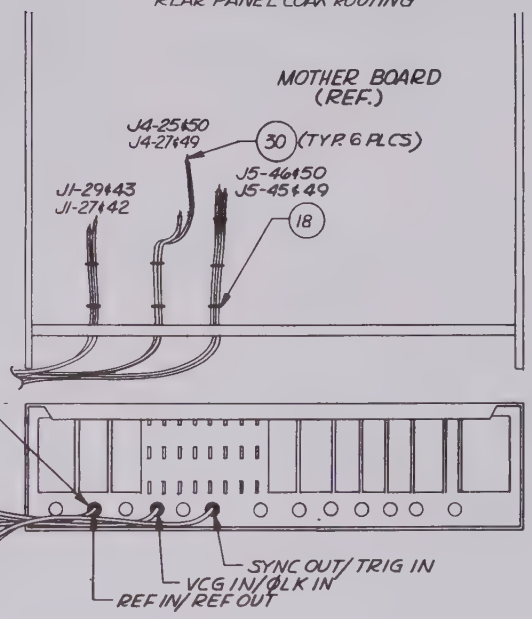
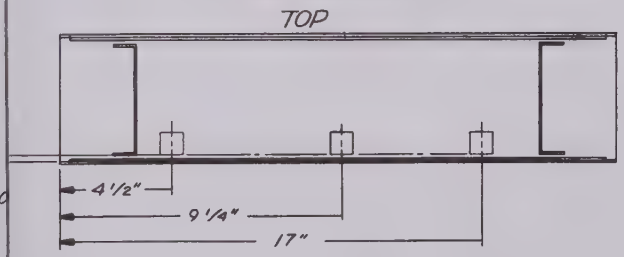
REV	ECN	BY	DATE	APP

DETAIL "A"
REAR PANEL COAX ROUTING



FUNCTION	COAX	SHIELD	COLOR	LENGTH (IN)
REF. IN	J1-29	J1-27	GRN	14"
REF. OUT	J1-43	J1-42	GRN/WHT	13"
VCG IN	J4-25	J4-27	RED/WHT	24"
BLK IN	J4-50	J4-49	BLK	15½"
SYNC OUT	J5-46	J5-45	BLU/WHT	17"
TRIG IN	J5-50	J5-49	BLU	17½"

DETAIL "B"
CABLE CLAMP LOCATION

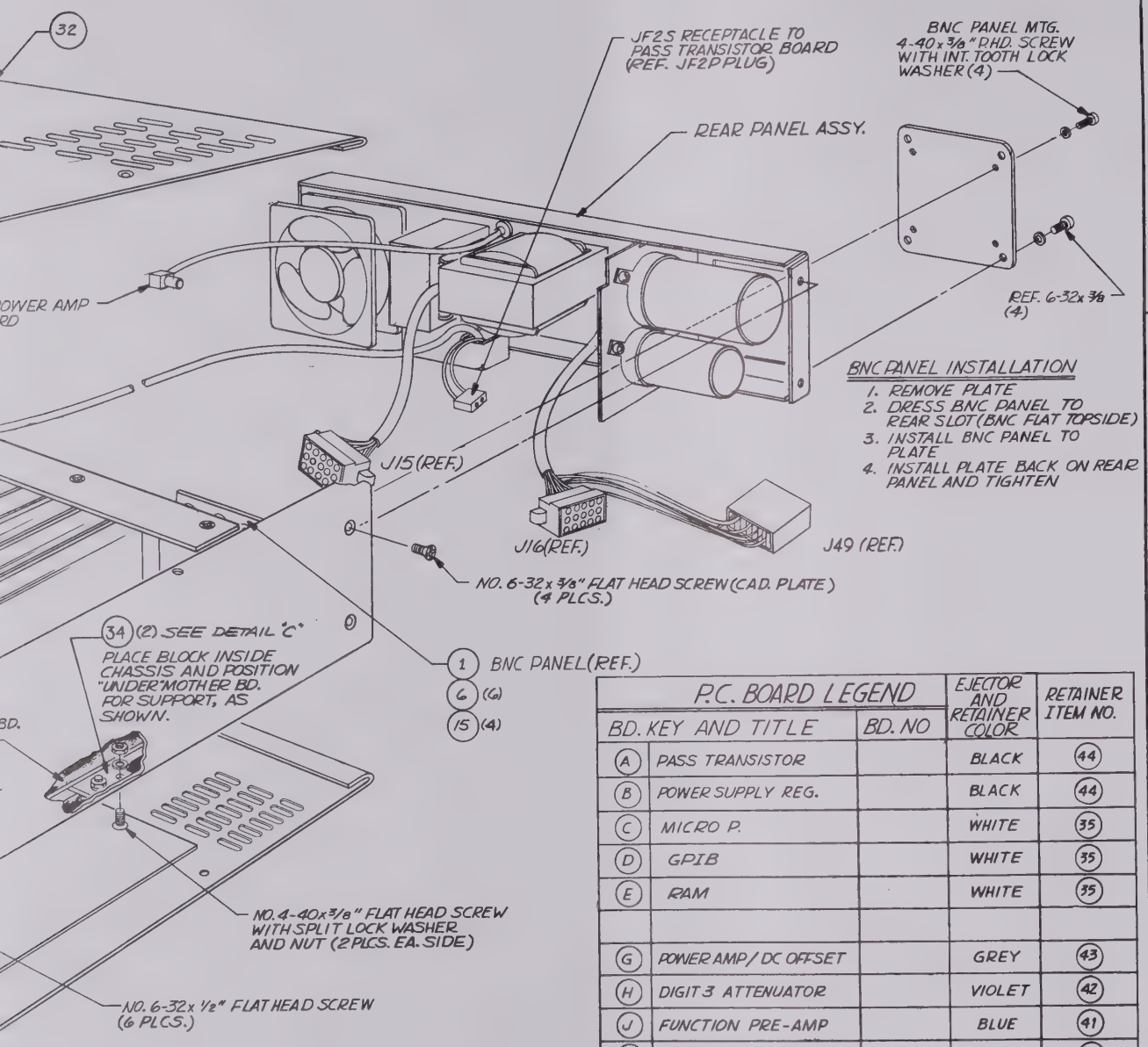


REV	ECN	BY	DATE	APP
G	2785	fma	9/17/14	
H	3553	DC	21-83	
/	3777 CLASS III	SC	9-22-83	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 7-25-7	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE ASSEMBLY CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 172 / DWG NO 0102-00-0726 / REV H
	SCALE		CODE IDENT 23338 / SHEET 1 OF 2

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP


32
JF2S RECEPTACLE TO PASS TRANSISTOR BOARD (REF. JF2P PLUG)
BNC PANEL MTG. 4-40 x 3/8" P.HD. SCREW WITH INT. TOOTH LOCK WASHER (4)
REAR PANEL ASSY.
REF. 6-32 x 3/8 (4)
BNC PANEL INSTALLATION
1. REMOVE PLATE
2. DRESS BNC PANEL TO REAR SLOT (BNC FLAT TOPSIDE)
3. INSTALL BNC PANEL TO PLATE
4. INSTALL PLATE BACK ON REAR PANEL AND TIGHTEN
J15 (REF.)
J16 (REF.)
J49 (REF.)
NO. 6-32 x 3/8" FLAT HEAD SCREW (CAD. PLATE) (4 PLCS.)
34 (2) SEE DETAIL "C"
PLACE BLOCK INSIDE CHASSIS AND POSITION "UNDER" MOTHER BD. FOR SUPPORT, AS SHOWN.
1 BNC PANEL (REF.)
6 (6)
15 (4)
NO. 4-40 x 3/8" FLAT HEAD SCREW WITH SPLIT LOCK WASHER AND NUT (2 PLCS. EA. SIDE)
NO. 6-32 x 1/2" FLAT HEAD SCREW (6 PLCS.)
33
9 (2 PLCS.)
PULL-UP TYP. BOTH ENDS
P.C. BD. EXTRACTED
P.C. BD. INSTALLED
CHASSIS EDGE (REF.)

DETAIL "D"
TYP. P.C. BD. REMOVAL

P.C. BOARD LEGEND			EJECTOR AND RETAINER COLOR	RETAINER ITEM NO.
BD. KEY	AND TITLE	BD. NO		
A	PASS TRANSISTOR		BLACK	44
B	POWER SUPPLY REG.		BLACK	44
C	MICRO P.		WHITE	35
D	GPIB		WHITE	35
E	RAM		WHITE	35
G	POWER AMP/DC OFFSET		GREY	43
H	DIGIT 3 ATTENUATOR		VIOLET	42
J	FUNCTION PRE-AMP		BLUE	41
K	TRIANGLE GENERATOR		GREEN	40
L	VCG		YELLOW	39
M	DIGIT 1/ MIXER		ORANGE	38
N	DIGIT 2 AND 3		RED	37
P	DIGIT 4 AND 5 / REF.		BROWN	36

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 7-25-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Salga	SEPT 1977	TITLE ASSEMBLY CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 172 / DWG NO 0102-00-07726 / REV H
	SCALE		CODE IDENT 23338 / SHEET 2 OF 2

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CABLE, 4 COND, 20GA	8722	BELDN	6001-70-0007	1

S	ASSEMBLY NO. 1101-00-0726 PAGE: 3	REV J

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN | DATE

PROJ ENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

PARTS LIST
CHASSIS

MODEL NO	DWG NO	REV
172B	1101-00-0726	J

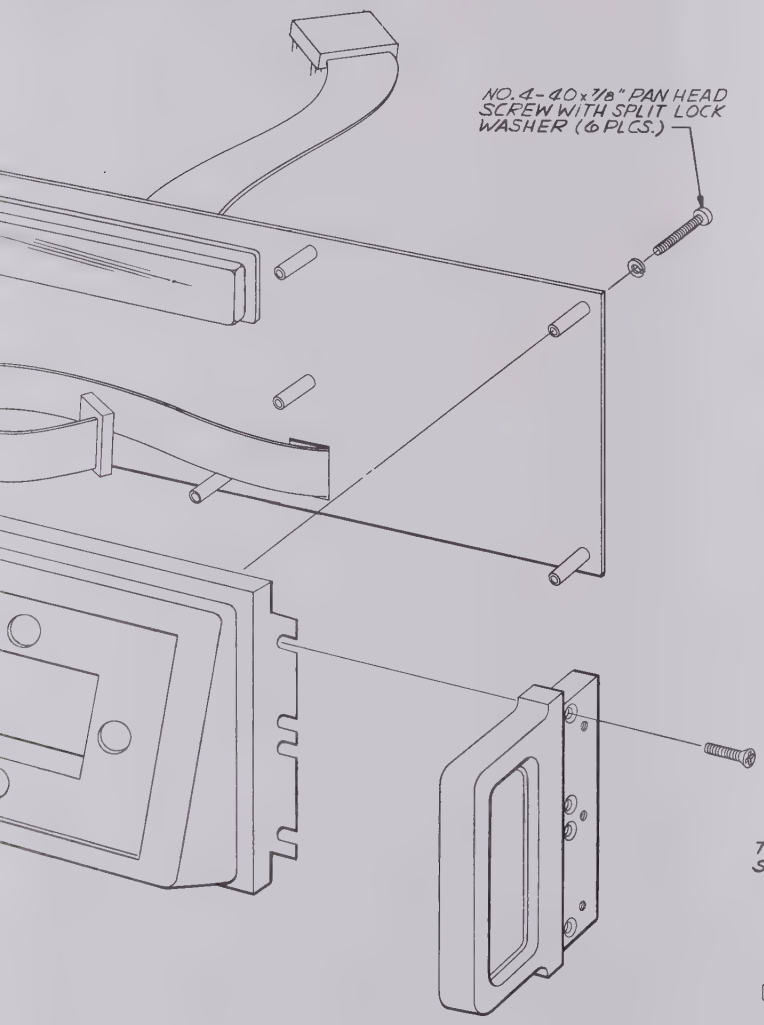
CODE IDENT 23338 | SHEET 1 OF 1

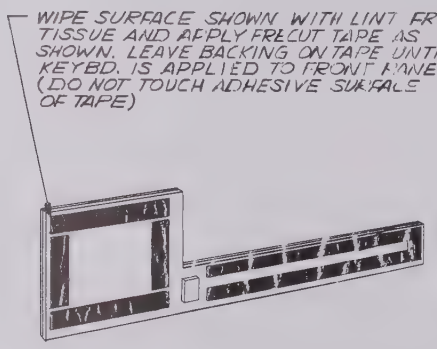
NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A 3894

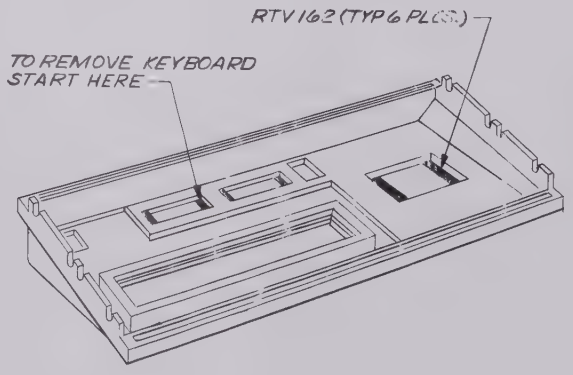
REV	ECN	BY	DATE	APP
	2982 CL III	fra	7/29/81	VNL

WIRE GA.	COLOR	DESTINATION
20	GRN	S1-2
20	BLK	S1-3
20	RED	S1-1
	NOT USED	
	NOT USED	
20	WHT	S1-4
20	GRN/YEL	SHIELD
	NOT USED	
	NOT USED	




WIPE SURFACE SHOWN WITH LINT FREE TISSUE AND APPLY PRECUT TAPE AS SHOWN. LEAVE BACKING ON TAPE UNTIL KEYBD. IS APPLIED TO FRONT PANEL. (DO NOT TOUCH ADHESIVE SURFACE OF TAPE)

DETAIL "A"



DETAIL "B"
KEYBOARD INSTALLATION
SEE NOTES 1 THRU 4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 6-20-80	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJENGR R.L. Schultz	9-17-81	TITLE ASSEMBLY FRONT PANEL	
	RELEASE APPROV			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030			
	DO NOT SCALE DWG		MODEL NO	DWG NO 0102-00-0968 REV
	SCALE		CODE IDENT 23338	SHEET / OF /

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REV	ECN	BY	DATE	APP

RT DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
SY DRWG, FRONT NEL	0102-00-0968	WVTK	0102-00-0968	1
ONT PANEL OM: 1400-00-7031	1400-00-7030	WVTK	1400-00-7030	1
NS, READOUT F: 3200-03-0007	1400-00-7680	WVTK	1400-00-7680	1
KT, SWITCH MTG.	1400-00-7703	WVTK	1400-00-7703	1
ATE, NAME	1400-00-8240	WVTK	1400-00-8240	1
SULATOR, PWR SWITCH F: 1600-99-0001	1400-00-8370	WVTK	1400-00-8370	2
ERLAY, KEYBOARD	1400-00-9790	WVTK	1400-00-9790	1
D., INSTRUMENT	1400-00-9800	WVTK	1400-00-9800	1
NDLE, WHITE OM: 1400-00-6951	1400-01-3152	WVTK	1400-01-3152	2
ITCH SUPPORT BD	1700-00-0750	WVTK	1700-00-0750	1
UG, 9PIN	03-06-2091	MOLEX	2100-02-0011	1
LDER LUG	1485-6	SMITH	2100-04-0025	1
N, MALE	02-06-2103	MOLEX	2100-05-0003	5
ITCH, POWER	5102-00-0006	WVTK	5102-00-0006	1
YBOARD	2SMD200P75079	CRL	5108-00-0003	1

NT PANEL	ASSEMBLY NO. 1101-00-0968 PAGE: 1	REV

RT DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
BLE, 4 COND, 20GA	8722	BELDN	6001-70-0007	1

NT PANEL	ASSEMBLY NO. 1101-00-0968 PAGE: 2	REV

OVE ALL BURRS
BREAK SHARP EDGES
RIAL
H
ETEK PROCESS

DRAWN | DATE
PROJ ENGR
RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ±.010 ANGLES ±1
XX ±.030

DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

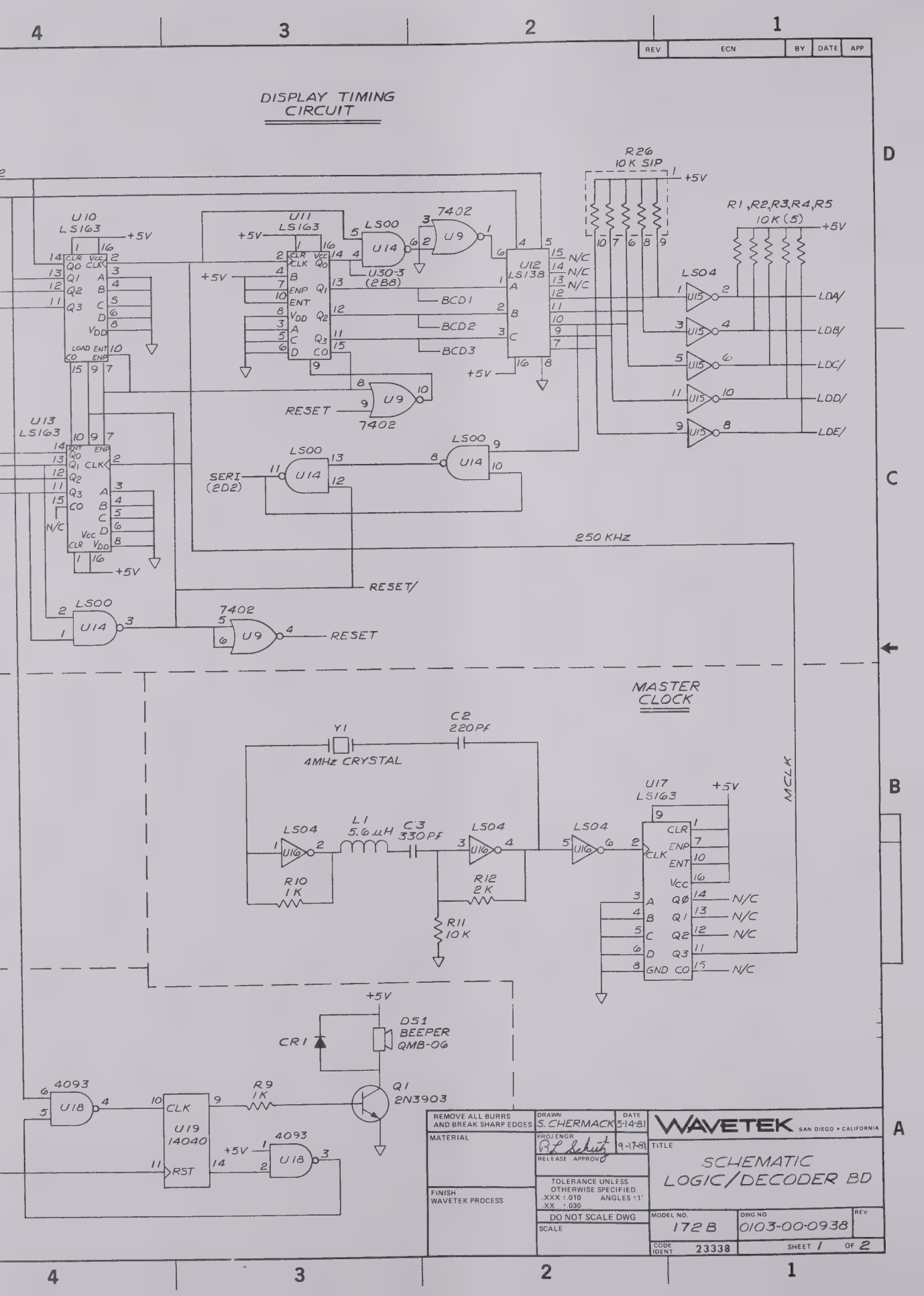
TITLE
PARTS LIST
ASSY, FRONT PANEL

MODEL NO	DWG NO	REV
172B	1101-00-0968	

CODE IDENT 23338 | SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-3894


REV
ECN
BY
DATE
APP
DISPLAY TIMING CIRCUIT
U10 LS163
U11 LS163
U12 LS138
U13 LS163
U14
U9
7402
LS00
LS04
R26 10K SIP
R1,R2,R3,R4,R5 10K (5)
+5V
BCD1
BCD2
BCD3
N/C
RESET
RESET/
SERI (2D2)
LDA/
LDB/
LDC/
LDD/
LDE/
250 KHz
MASTER CLOCK
Y1
4MHz CRYSTAL
C2 220pf
L1 5.6 µH
C3 330pf
R10 1K
R11 10K
R12 2K
U17 LS163
MCLK
CR1
D51 BEEPER QMB-06
Q1 2N3903
R9 1K
4093
U18
U19 14040
CLK
RST
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S. CHERMACK 5-14-81
PROJ ENGR 9-17-81
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC LOGIC/DECODER BD
MODEL NO. 172B
DWG NO 0103-00-0938
REV
CODE IDENT 23338
SHEET 1 OF 2

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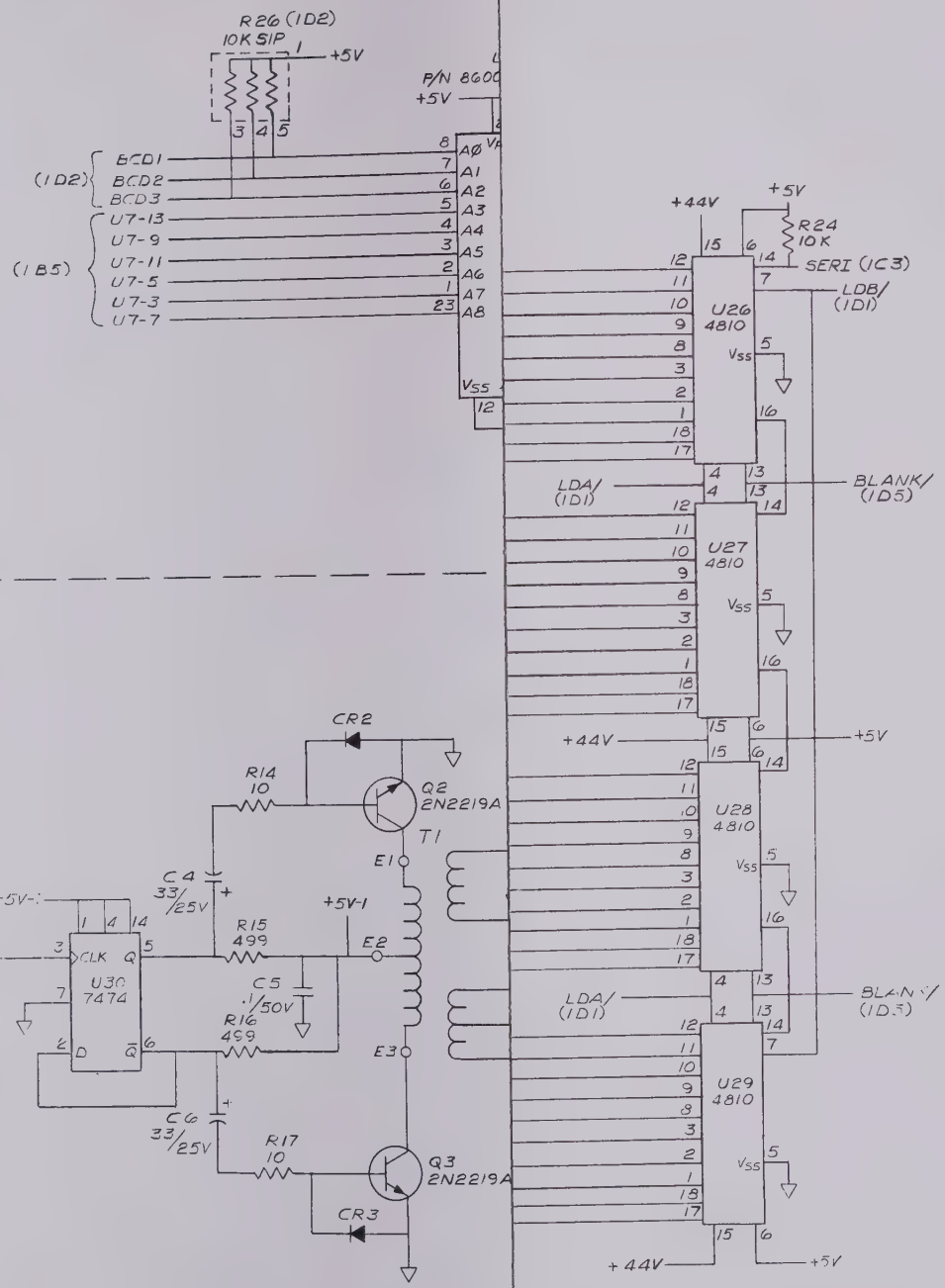
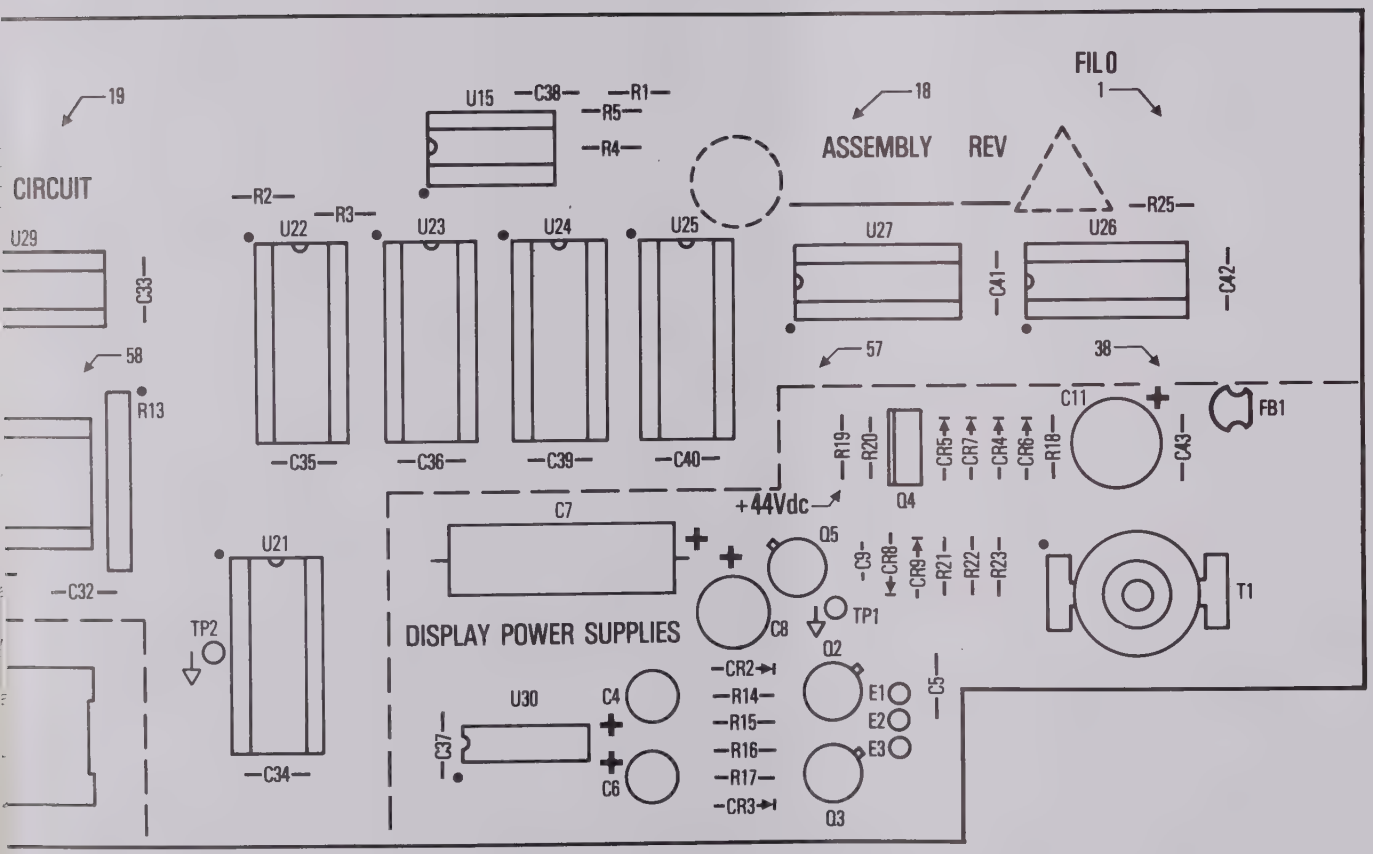
REV	ECN	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 5-14-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR R L Schuth	9-17-81	TITLE SCHEMATIC LOGIC/DECODER BD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		MODEL NO. 172B
	DO NOT SCALE DWG		DWG NO. 0103-00-0933 REV
	SCALE		CODE IDENT 23338 SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PCA LOGIC/DECODER
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ·010 ANGLES ·1 XX ·030		
	DO NOT SCALE DWG		MODEL NO 172 B / DWG NO 0101-00-0938 / REV
	SCALE		CODE IDENT 23338 / SHEET OF

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PAR
NONE	ASSY DRWG, LOGIC/ DECODER BOARD	0101-00-0938
NONE	SCHEMATIC, LOGIC/ DECODER BOARD	0103-00-0938
NONE	TRANSFORMER	172B-0030
C9	CAP, CER, .001MF, 1KV	DD-102
C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C5	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z0
C10	CAP, CER, .022MF, 25V	HY-525
C3	CAP, CER, 330PF, 1KV	DD-331
C1	CAP, CER, 47PF, 1KV	DD-470
C2	CAP, MICA, 220PF, 500V	DM15-221J
C7	CAP, ELECT, 4MF, 350V	TVA-1601
C11	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	CRE SERIES 10
C4 C6	CAP, ELECT, 33MF, 25V RADIAL LEAD, SP .14	CLE-L SERIES
C8	CAP, ELECT, 47MF, 50V	CRE SERIES 47

WAVETEK PARTS LIST | TITLE PCA, LOGIC/DECODER BD | ASS 11 | PA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PAR
	RADIAL LEAD, SP .20	
NONE	LOGIC/DECODER BOARD	1700-00-0938
L1	CHOKE, 5.6MH	1537-30
NONE	SKT, IC, 24PIN	DILB-24P-108
NONE	SKT, IC, 40PIN	DILB-40P-108
NONE	SOCKET, 14 PIN	C8814-01
NONE	SKT, IC, 22 PIN	DILB-22P-108
1	SKT, IC, 24 PIN	CA-24SPU-10SD
2	LOCK, SOCKET	CA-24-200-DL
NONE	SOCKET, 18 PIN	DIBL-18P-108
TP1 TP2 TP3	BUSS BAR STANDOFF	2110-001
Y1	CRYSTAL, 4MHZ	180-502
V1	DISPLAY, FLOUR. (40 CHARACTER)	DC405A2
NONE	SPACER, SWAGE .500 H, .250 DIA .150DIA THRU, .062MTL	6310-1/2-2-C
NONE	SPACER, SWAGE .750 H, .250 DIA .150DIA THRU, .062MTL	6310-3/4-2-C

WAVETEK PARTS LIST | TITLE PCA, LOGIC/DECODER BD | ASS 11 | PAG

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC	74LS138	TI	8007-41-3810	1
IC	74LS163	SIG	8007-41-6310	4
IC	74LS240	TI	8007-42-4010	1
IC	74LS368	TI	8007-43-6810	2
IC, PROGRAMMED REF: 8000-27-1600	8600-00-0224	WVTK	8600-00-0224	1

GIC/DECODER BD | ASSEMBLY NO. 1100-00-0938 | PAGE: 5 | REV

NOTE UNLESS OTHERWISE SPECIFIED

EMOVE ALL BURRS ND BREAK SHARP EDGES
TERIAL
UISH VETEK PROCESS

DRAWN | DATE
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

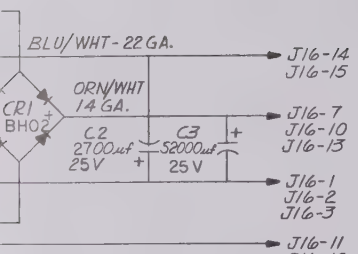
TITLE
PARTS LIST
PCA, LOGIC/DECODER BD

MODEL NO	DWG NO	REV
172B	1100-00-0938	
CODE IDENT 23338	SHEET 1 OF 1	

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894

REV	ECN	BY	DATE	APP
A	ECN 2785	fm	9/17/81	DTB

J16-4 ⟩——⟨ J49-8
J16-5 ⟩——⟨ J49-2
J16-6 ⟩——⟨ J49-1

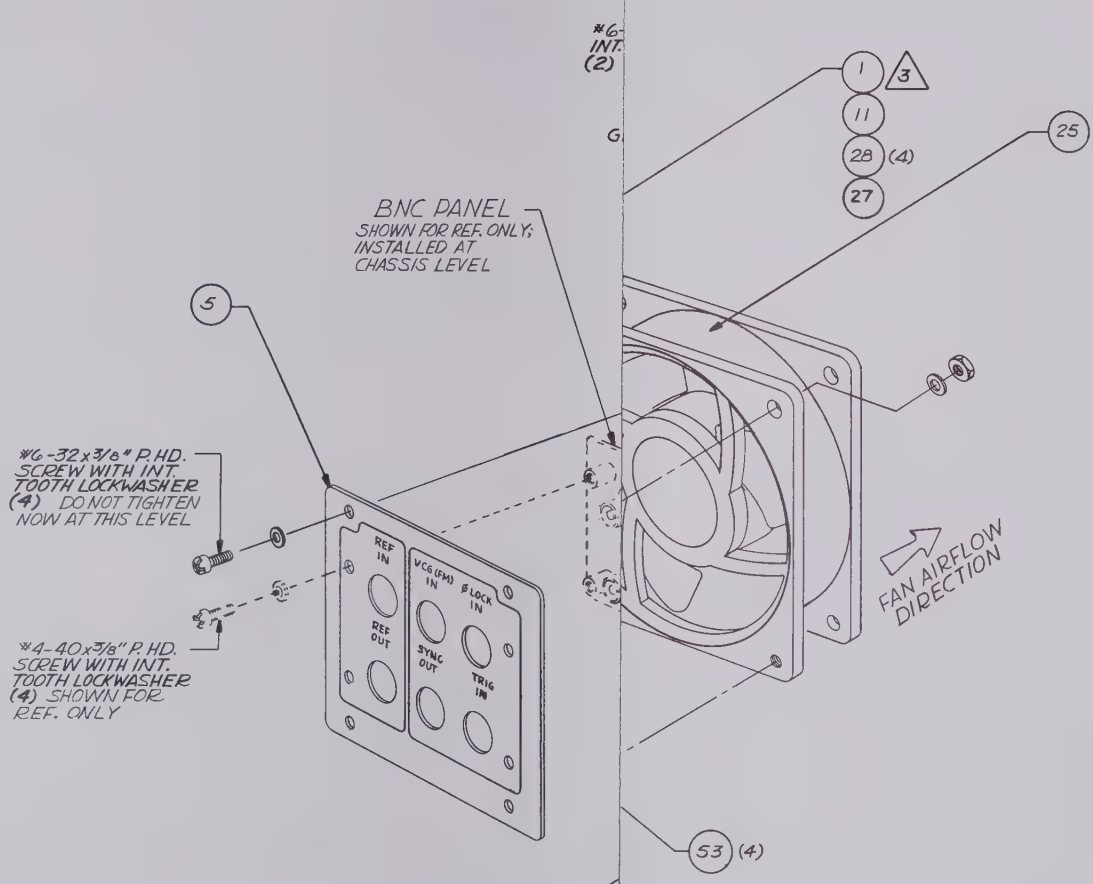


J16-14
J16-15
J16-7
J16-10
J16-13
J16-1
J16-2
J16-3
J16-11
J16-12
J16-8
J16-9
15 VAC
J15-14
J15-15
15 V COM
J15-8
J15-9
15 VAC
J15-11
J15-12
24 VAC
J15-2
J15-5
24 V COM
J15-1
J15-4
24 VAC
J15-3
J15-6

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 6-9-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC POWER SUPPLY AND REGULATOR REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO. / DWG NO. 0104-00-0792 / REV. A
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
A	ECN # 2132	LJTE	5-5-81	
B	ECN * 2375	DC	10/10/80	
C	ECN 2785	fra	9/17/81	
D	ECN 2966	fra	1/12/82	
	ECN 2977 (CL III)	fra	3/9/82	
	3227 (CL III)	fra	6/5/82	


*6-32 INT. (2)
1
3
11
28 (4)
27
25
BNC PANEL
SHOWN FOR REF. ONLY; INSTALLED AT CHASSIS LEVEL
5
*6-32 x 3/8" P. HD. SCREW WITH INT. TOOTH LOCKWASHER (4) DO NOT TIGHTEN NOW AT THIS LEVEL
*4-40 x 3/8" P. HD. SCREW WITH INT. TOOTH LOCKWASHER (4) SHOWN FOR REF. ONLY
REF IN
REF OUT
VCG (FM) IN
SYNC OUT
Ø LOCK IN
TRIG IN
FAN AIRFLOW DIRECTION
53 (4)
*8-32 x 1/4" SCREW WITH INT. TOOTH LOCKWASHER (8) (USED ON T1 AND T2)
SHOULDER
6-32 x 1/2" PAN HEAD SCREW WITH INTERNAL TOOTH LOCK WASHER AND NUT (2)
*6-32 x 3/8" SCR
INT. TOOTH LOCKW

3. SECURE T1 AND T2 TO PANEL BEFORE TIGHTENING BRACKET SCREWS

2. COMPLETE WIRING PRIOR TO INSTALLATION OF CAPACITOR ASSEMBLY TO REAR PANEL

1. INSTALL ITEM 20 INTO POSITION AS SHOWN. SELF RETAINERS WILL SECURE ITS POSITION WITHIN THE PANEL

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS

DRAWN D. COOPER 6-6-77
PROJ ENGR Tom Saliga 6-21-77
RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ± .010 ANGLES ±1
.XX ± .030

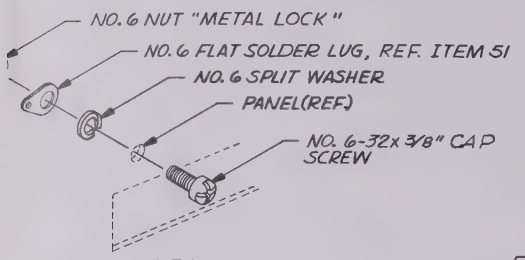
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
ASSEMBLY REAR PANEL

MODEL NO.
DWG NO. 0102-00-0792
REV D
CODE IDENT 23338
SHEET 1 OF 3

REV	ECN	BY	DATE	APP



DETAIL "B"
TYP. GROUND LUG STACK-UP
(3 PLACES)

NOTE: ALL CONNECTORS TO BE MECHANICALLY SECURE TO CHASSIS PRIOR TO SOLDERING GROUND WIRES TO LUGS.

ADD SHRINK SLEEVING (1.5" LONG) TO TERMINALS (4 PLCS) USE NO. 10-32 x 5/8" P. HD. SCREW WITH LOCK WASHERS UNDER AND ON TOP OF LUG (TYP. 4)

WHT (4) (3)18GA, (1)14GA

ORN(4) (1)14GA, (3)18GA

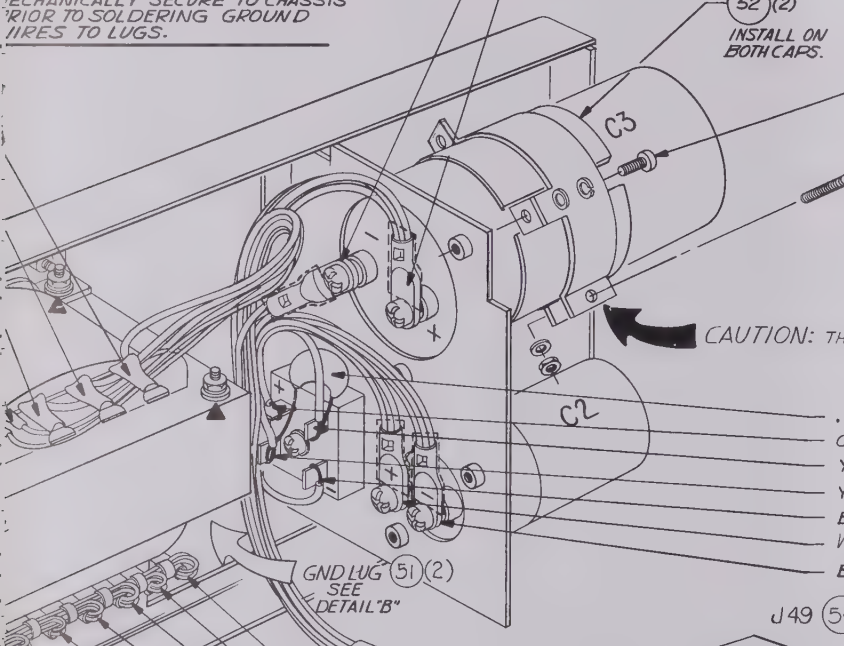
(22) (4)

(52) (2) INSTALL ON BOTH CAPS.

NOTE: ASSEMBLE CAPACITOR BRACKETS (2) COMPLETELY BEFORE MOUNTING TO REAR PANEL

* 6-32 x 3/8" SCREW WITH FLAT WASHER AND SPLIT LOCK WASHER (5)

*8-32 x 5/8" P.HD. SCREW WITH LOCKWASHER AND NUT (2)


C3
C2
CAUTION: THIS TAB MUST BE IN LOCATION SHOWN
.1/50V CAPACITOR (C1)
ORN
YEL/WHT
YEL/WHT
BLU
WHT (2) - (1)14 GA (1)18 GA
BLU(3) - - (1)14GA (2)18 GA
(31) (CR1, REF.)
INSTALL BRIDGE ASSY. WITH *6-32 x 5/8" SCREW WITH INT. TOOTH LOCKWASHER (USE HEATSINK COMPOUND)
GND LUG (51) (2) SEE DETAIL "B"

J49 (54) (55) (6)

3/8" SLEEVING

FOR DETAIL WIRING OF J16 AND J49 SEE SHT 3 of 3

[1] BLK, BLK, YEL/WHT
[2] ORN, ORN
[3] VIO/WHT, BLK/WHT, BLK/WHT
[4] GRY, GRY
[5] GRY/WHT, GRY/WHT
[6] GRN/YEL TO T1
[6] GRN/YEL TO GRND LUG #2

J16
(17) (24) (10)

NOTE: ADD NUMBER STICKERS TO J15 AND J16

(18) SEE DETAIL "C"

#4 SLEEVING

(12) (24) (17) J15

PIN NO.	WIRE COLOR	GA.
1	BLU/WHT	22
2	BLU	
3	BLU	
4	BLU/WHT	
5	BLU	
6	BLU	
7	NOT USED	
8	WHT/GRN	
9	WHT/GRN	
10	NOT USED	
11	GRN	
12	GRN	
13	NOT USED	
14	GRN	
15	GRN	22

(16) (23) (5)

SEE DETAIL "A" (CORCOM WIRING)

JUMPERS REQ'ED.
PIN 1 TO 4 BLU/WHT
2 5 BLU
3 6 BLU
8 9 WHT/GRN
11 12 GRN
PIN 14 TO 15 GRN

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 6-6-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Salga.	6-21-77	TITLE ASSEMBLY REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO
	SCALE		DWG NO 0102-00-0792 REV D
	CODE IDENT 23338		SHEET 2 OF 3

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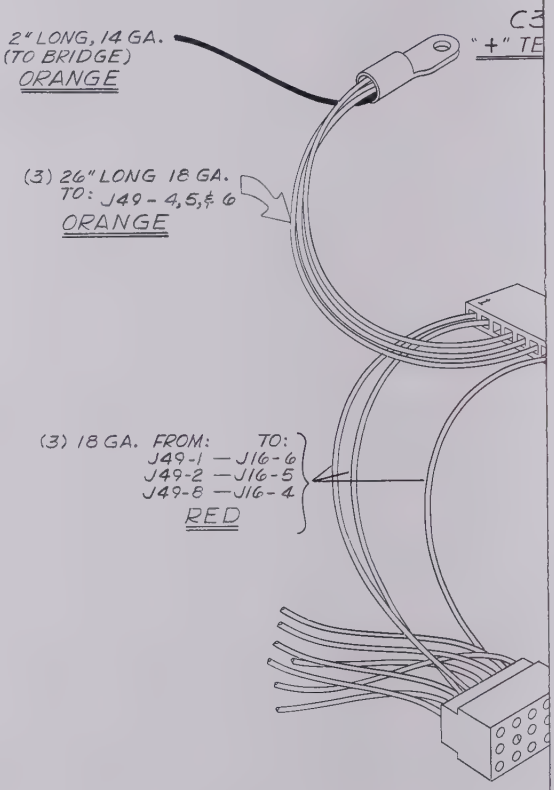
REV	ECN	BY	DATE	APP



J49 WIRING

PIN NO.	DESTINATION	COLOR	GA.
1	J16-6	RED	18
2	J16-5	RED	18
3	NOT USED		
4	"+" C3	ORN	18
5	"+" C3	ORN	18
6	"+" C3	ORN	18
7	NOT USED		
8	J16-4	RED	18

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS

DRAWN RO FIFER DATE 3-1-78
PROJ ENGR
RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ±1
.XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
ASSEMBLY
REAR PANEL

MODEL NO
DWG NO. 0102-00-0792 RF D
CODE IDENT 23338
SHEET 3 OF 3

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
33	BNC CONN	KC-19-152	KING	2100-01-0006	1
16	CONN, 9PIN	03-06-1091	MOLEX	2100-02-0010	1
3	CONN, 15PIN	03-09-1151	MOLEX	2100-02-0012	1
17	PLUG, 15PIN	03-09-2151	MOLEX	2100-02-0013	2
54	CONN HOUSING	1-87025-6	AMP	2100-02-0077	1
NONE	CONNECTOR	JF2S	WINCH	2100-02-0081	1
20	RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
22	LUG	35	ILSCO	2100-04-0018	4
51	SOLDER LUG	1485-6	SMITH	2100-04-0025	2
23	PIN, FEMALE	02-06-1103	MOLEX	2100-05-0002	5
24	PIN, MALE	02-09-2118	MOLEX	2100-05-0005	22
55	CONN PINS	87027-3	AMP	2100-05-0047	6
18	CONN	27-843	AMPH	2100-07-0009	1
47	LABEL, RECEPT	85-1505	CORCM	2400-04-0001	1
NONE	FUSE, 3A, 250V	312003	LITFU	2400-05-0018	1
8	FAN FILTER	3502	PAMOT	2600-01-0005	1
25	FAN, MODIFIED	2600-99-0002	WVTK	2600-99-0002	1

WAVETEK PARTS LIST	TITLE REAR PANEL ASSY	ASSEMBLY NO. 1101-00-0792 PAGE: 2	REV C

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
0102-00-0792	WVTK	0102-00-0792	1
0104-00-0792	WVTK	0104-00-0792	1
172B-0035	WVTK	1204-00-0035	1
172B-0054	WVTK	1204-00-0054	1
1400-00-6210	WVTK	1400-00-6210	1
1400-00-7043	WVTK	1400-00-7043	1
1400-00-7523	WVTK	1400-00-7523	1
1400-00-7543	WVTK	1400-00-7543	4
1400-00-7783	WVTK	1400-00-7783	2
1400-00-7790	WVTK	1400-00-7790	1
1400-00-7810	WVTK	1400-00-7810	1
1400-00-8880	WVTK	1400-00-8880	1
1400-00-9090	WVTK	1400-00-9090	1
1400-01-3191	WVTK	1400-01-3191	2
CAC03Z5U104Z050A	CORNG	1500-01-0405	1
91C25HA272	MEPCO	1500-32-7202	1
FAHM52000-15-B3	CDE	1500-35-2301	1

ASSEMBLY NO. 1101-00-0792 PAGE: 1	REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	FROM: 2600-00-0005				
46	TIE MOUNT	TM-256C	PANDT	2800-00-0005	1
NONE	TY-WRAP	TY-523M	TB	2800-00-0006	20
27	INSERT # 6	74-11-106-13	SOTCO	2800-09-0017	12
28	INSERT #8	74-11-108-13	SOTCO	2800-09-0018	8
29	CAP, MTG, BKT	FJMR	STM	2800-12-0006	1
30	CAP, MTG, BKT	FHMR-2	STM	2800-12-0007	1
53	NUT, PRESS, 6-32	S-632-1	PEM	2800-16-0014	4
34	WASHER, SHOULDER	2668	SMITH	2800-27-0004	1
35	NYLON FLAT WASHER	2264-N-385	AMTOM	2300-28-0005	1
40	SLEEVING, BLK 3/8 IN.	SLEEVING, BLACK 3/8"	NATBR	3000-00-0024	2
41	SLEEVING, BLACK #4	SLEEVING, BLACK #4	NATBR	3000-00-0025	2
42	SLEEVING, BLACK #8	SLEEVING, BLACK #8	NATBR	3000-00-0026	2
31	BRIDGE ASSY 30 AMP	MDA990-1	MOT	4899-00-0010	1
NONE	CABLE, 4 COND, 20GA	8722	BELDN	6001-70-0007	1

WAVETEK PARTS LIST	TITLE REAR PANEL ASSY	ASSEMBLY NO. 1101-00-0792 PAGE: 3	REV C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
	RELEASE APPROV		PARTS LIST REAR PANEL ASSY
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 172B / DWG NO. 1101-00-0792 / REV C
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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REV	ECN	BY	DATE	APP
A	"P17" WAS "J1", J1 WAS J2, "NDAC" WAS "NOAC", "AD1Ø/" THRU "AD1Ø/" WAS "AQ1Ø/" THRU "AQ14/"	TLF	6-30-77	
B	ECN 1687	RO	3-22-78	
C	ECN 2487	LOU	1-19-81	

GP
PI

⚠ GREEN WIRE TO CHASSIS GROUND

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN T. FOSTER DATE 5/16/77

PROJ ENGR Tom Daiga SEPT 6 '77

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ±.010 ANGLES ±1
XX ±.030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC -
GPIB DECODER

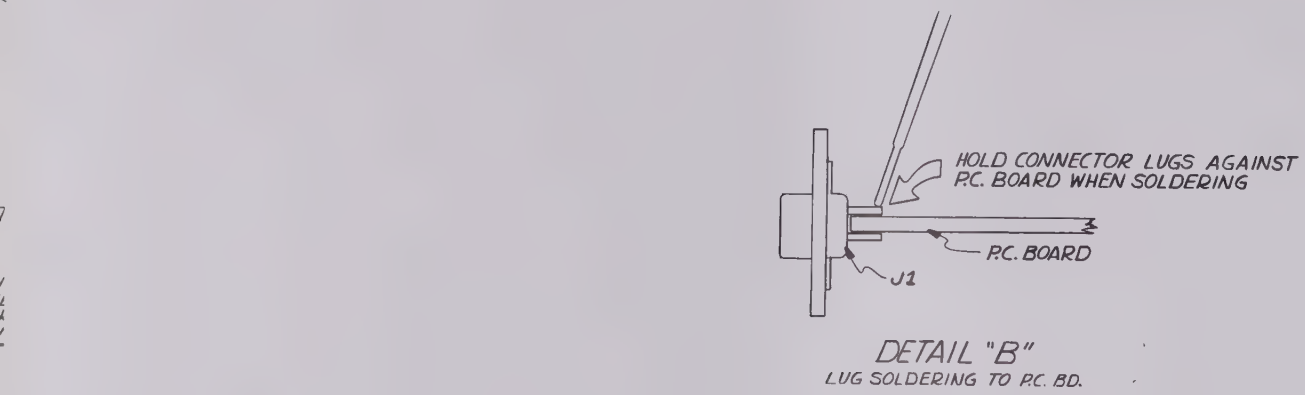
MODEL NO.

DWG NO. 0103-00-0554

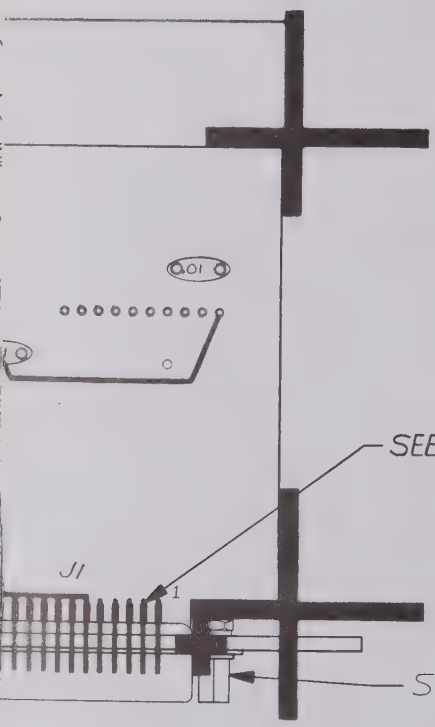
REV C

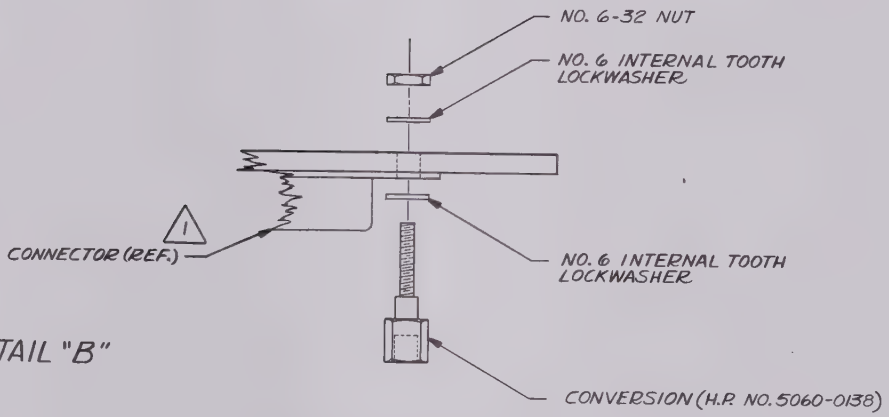
CODE IDENT 23338

SHEET 1 OF 1

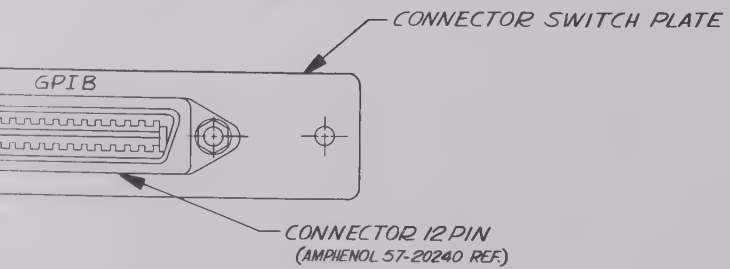


DETAIL "B"
LUG SOLDERING TO P.C. BD.





DETAIL "A"
H.P. CONVERSION NO. 5060-0138
HP-IB



K	# 2487	LOU	1-19-81
J	# 2129	LJTE	4-30-80
H	# 2039	[illegible]	8-28-79
G	ECN 593	DC	11-10-78
F	ECN 1687	RJ	5-29-78

DRAWN	D. COOPER	DATE 11-8-76
PROJ ENGR	Tom Saliga	SEPT 6 '77
RELEASE APPROV		

WAVETEK

ASSEMBLY
GPIB DECODER

0101-00-0554 K

SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
DRWR DECODER	0101-00-0554	WVTK	0101-00-0554	1
MATIC DECODER	0103-00-0554	WVTK	0103-00-0554	1
. BLOCK	157-314	WVTK	1400-00-3043	1
PLATE	1400-00-6610	WVTK	1400-00-6610	1
CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNR	1500-01-0310	2
DER	1700-00-0554	WVTK	1700-00-0554	1
	57-20240	AMPH	2100-02-0060	1
ET	516-A07D	AUGAT	2100-03-0034	1
LOCK LUG	1414-6	SMITH	2100-04-0009	1
SCREW	408-146475	AMPH	2800-23-0008	2
CH PC	500-105	DUNCN	5179-00-0001	1
RCONNECT CABLE	CA-D24P02-26-1TT-016	CA	6002-00-0002	1

EAR INTERF	ASSEMBLY NO. 1100-00-0554 PAGE. 1	REV H

REMOVE ALL BURRS AND BREAK SHARP EDGES

ATERIAL

NISH AVETEK PROCESS

DRAWN | DATE

PROJ ENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

PARTS LIST
PCA, GPIB REAR INTERF

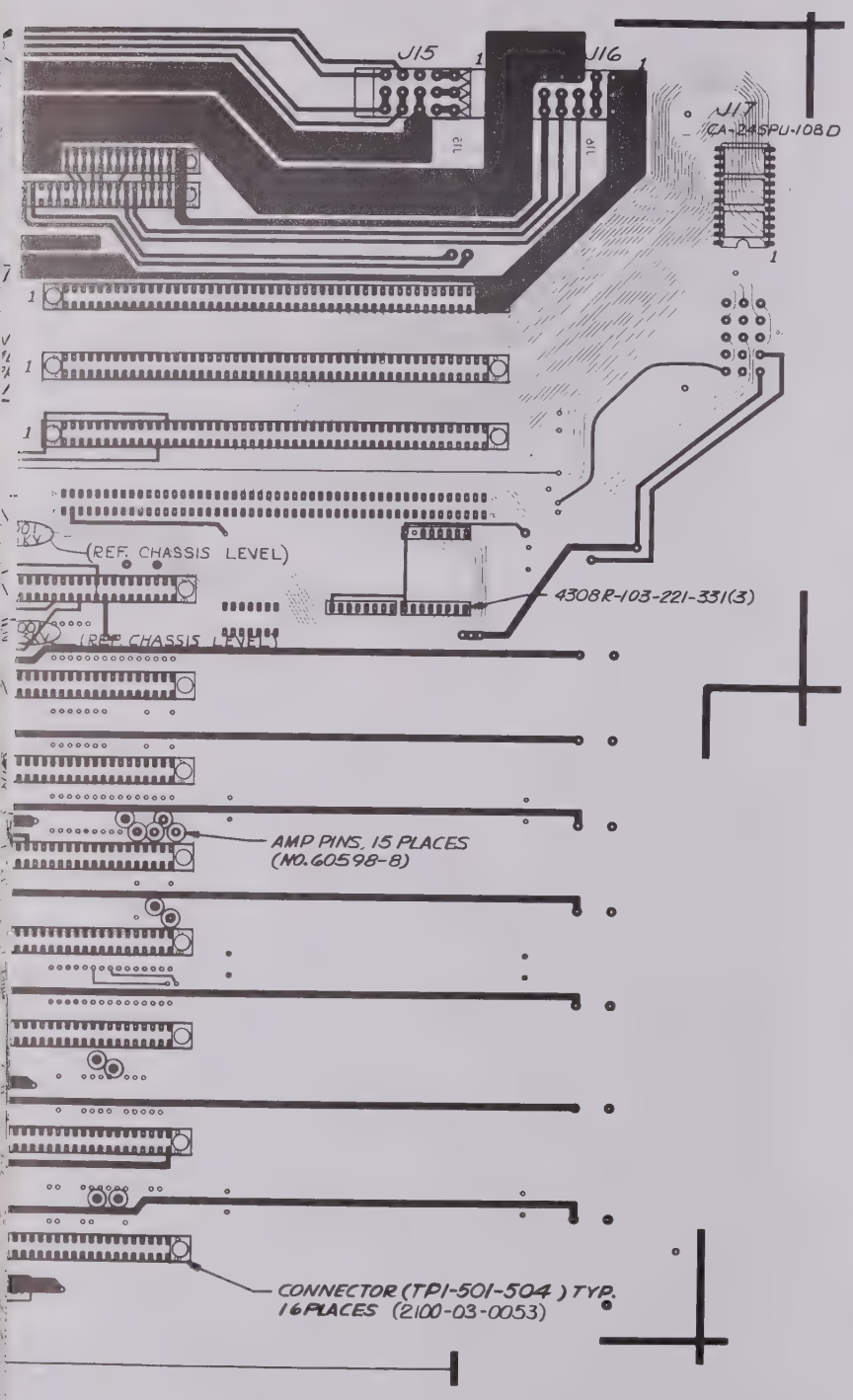
MODEL NO	DWG NO	REV
172B	1100-00-0554	H

CODE IDENT 23338 SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894

REV	ECN	BY	DATE	APP
B	ECN 1689	RO	3-14-78	
C	ECN 1844	RO	11-16-78	
D	ECN 1941	DC	3-22-79	
E	ECN 2131	LJTE	5-1-80	



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 9-4-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Saliga	SEPT 6'77	TITLE ASSEMBLY MOTHER BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO	DWG NO 0101-00-0717 REV E
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
ASBY DRWG MOTHER	0101-00-0717	WVTK	0101-00-0717	1
CAP, ELECT, 250MF, 16V	500D257G016DF7	SPRAG	1500-32-5101	5
MOTHER BOARD	1700-00-0651	WVTK	1700-00-0651	1
CONN, 15PIN	03-09-1151	MOLEX	2100-02-0012	2
SKT, IC, 24 PIN	CA-24SPU-10SD	CA	2100-03-0045	2
CONN, EDGE CARD-GP	TP1-501-504	TEKA	2100-03-0053	16
PIN, FEMALE	02-09-1133	MOLEX	2100-05-0004	30
CONN	60598-8	AMP	2100-05-0017	17
STANDOFF, SWAGE .125 H, .250 DIA 4-40, .093 MAT'L	6911-2-3C	LYNTR	2800-03-0003	2
RES MODULE	4308R-103-221/331	BOURN	4770-00-0013	15
DIODE	1N746A	FAIR	4801-01-0746	1

THER BD	ASSEMBLY NO. 1100-00-0717 PAGE: 1	REV B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, MOTHER BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 172B	DWG NO 1100-00-0717 REV B
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A 3894

No Connector

J10/Memory RAM

B Side	Pin	A Side
±5V GND	1, 2	±5V GND
+12V	3	+12V
	4	
DBUS0/	5	DBUS1/
DBUS2/	6	DBUS3/
DBUS4/	7	DBUS5/
DBUS6/	8	DBUS7/
	9	
OPACK/	10	OPREQ/
M/$\overline{IO}$	11	E/NE
$\overline{RD}$/WT	12	WRP
	13	RDMA/
INTREQ/	14	INTACK
FLAG/	15	SENSE/
MRST/	16	RUN/$\overline{WAIT}$
WIOD/	17	RIOD/
	18	
OPREQ	19	WRPS
	20	
	21	
RDKYBD/, KBOUT/ KBIN/	22	DISPEN/
	23	
	24	
	25	
	26	
SYS CLK 5	27	SYS CLK 4
SYS CLK 3	28	SYS CLK 2
SYS CLK 1	29	SYS CLK 0
	30	
	31	
	32	
CO7	33	STRB/
CO6	34	A3/
CO5	35	A2/
CO4	36	A1/
CO3	37	A0/
CO2	38	XSGN/
CO1	39	D7/
CO0	40	D6/
CI7	41	D5/
CI6	42	D4/
CI5	43	D3/
CI4	44	D2/
CI3	45	D1/
CI2	46	D0/
CI1	47	CI0
	48	
+5V TTL	49, 50	+5V TTL
+5V TTL	51, 52	+5V TTL
-5V	53	-5V
	54	
	55	
	56	
	57	
	58	
	59	
	60	
	61	
+5V ISO COM	62	+5V ISO COM
+5V ISO	63	+5V ISO
	64	
	65	
	66	
MRST	67	MRST/
	68	
	69	
	70	
	71	
	72	
	73	
	74	
	75	
	76	
+5V ISO COM	77	+5V ISO COM
DIO8	78	+5V ISO
DIO2	79	DIO3
DIO7	80	DIO1
DIO6	81	DIO5
DIO4	82	SRQ
NDAC	83	NRFD
REN	84	
	85	
	86	ATN
IFC	87	DAV
EOI	88	
	89	
ABUS14/	90	ABUS15/
ABUS12/	91	ABUS13/
ABUS10/	92	ABUS11/
ABUS8/	93	ABUS9/
ABUS6/	94	ABUS7/
ABUS4/	95	ABUS5/
ABUS2/	96	ABUS3/
ABUS0/	97	ABUS1/
	98	
±5V GND	99, 100	±5V GND

J11/GPIB Interface
(Same as J10)

J12/Microprocessor
(Same as J10)

J8/Power Amplifier/DC Offset

B Side	Pin	A Side
C07	1	Strobe
C06	2	A3
C05	3	A2
C04	4	A1
C03	5	A0
C02	6	XSGN
C01	7	D7
C00	8	D6
C17	9	D5
C16	10	D4
C15	11	D3
C14	12	D2
C13	13	D1
C12	14	D0
C11	15	CI0
GND	16	XRD.
	17	
	18	
+5V	19, 20	+5V
	21	
±5V GND	22, 23, 24	±5V GND
A	25	A
±15V GND	26, 27, 28	±15V GND
	29	
15V	30, 31	−15V
	32	
+15V	33, 34	+15V
	35	
24V	36, 37	−24V
	38	
+24V	39, 40	+24V
	41	
−5V	42	−5V
	43	
±24 GND (±24 CT XFMR)	44, 45, 46, 47	±24 GND (±24 CT XFMR)
	48	
	49	
	50	

J13/Power Supply Regulator

B Side	Pin	A Side
OUT	1	IN
OUT	2	IN
±15V	3	±15V
AC	4	AC
+12V	5	+12V
	6	
±15, ±12 COM	7, 8, 9, 10, 11	±15, ±12 COM
B	12	B
C	13	C
E	14	E
−15V	15, 16	−15V
B	17	B
C	18	C
E	19	E
+15V	20, 21	+15V
B	22	B
C	23	C
E	24	E
−24V	25, 26	−24V
B	27	B
C	28	C
E	29	E
+24V	30, 31	+24V
±24 VAC	32	±24 VAC
	33	
	34	
±24 V COM	35, 36	±24 V COM
	37	
+5D	38	+5D
+5S	39	+5S
+5V	40, 41	+5V
±5V COM	42, 43	±5V COM
ISO AC From Xfmr	44, 45	ISO AC From Xfmr
−5V	46	−5V
ISO IN	47	ISO IN
ISO COM	48	ISO COM
ISO +5V	49	ISO +5V
−5V IN From Diode Bridge	50	−5V IN

J14/Pass Transistor/Regulator

B Side	Pin	
IN	1	High Voltage
IN	2	
±15V	3	
AC	4	
	5	
+12V	6	
	7	
±15V	8	
CT	9	
	10	
B	11	
C	12	
	13	
E	14	
	15	
	16	
B	17	
C	18	
E	19	
	20	
B	21	
C	22	
	23	
E	24	
	25	
B	26	
C	27	
	28	
E	29	
	30	
+5V IN TIP 29-C	31, 32, 33, 34, 35	To "+" of 18,000 µF
	36	
TIP 29-B	37	
TIP 35-E	38	
+5V	39, 40, 41, 42, 43	
±5V COM	44, 45	
5V	46	
ISO IN	47	
ISO COM	48	
ISO +5V	49	
5V IN	50	

J15, 15V & 24V TRANSFORMER

- 1, 4 — 24V Common
- 2, 5 — 24 Vac
- 24V Winding
- 3, 6 — 24 Vac
- 8, 9 — 15V Common
- 11, 12 — 15 Vac
- 15V Winding
- 14, 15 — 15 Vac

J16, 5V TRANSFORMER

- 1, 2, 3 — Digital Common
- 8, 9 — 5V ISO
- 11, 12 — 5V ISO
- AC Winding
- 14, 15 — 5V Unregulated

J49

- 4, 5, 6 — +5V Unregulated

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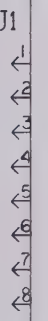
REV	ECN	BY	DATE	APP
A		TLF	6-24-77	
B	ECN 1687	RO	3-23-78	
C	ECN 1897	CC	4-25-79	

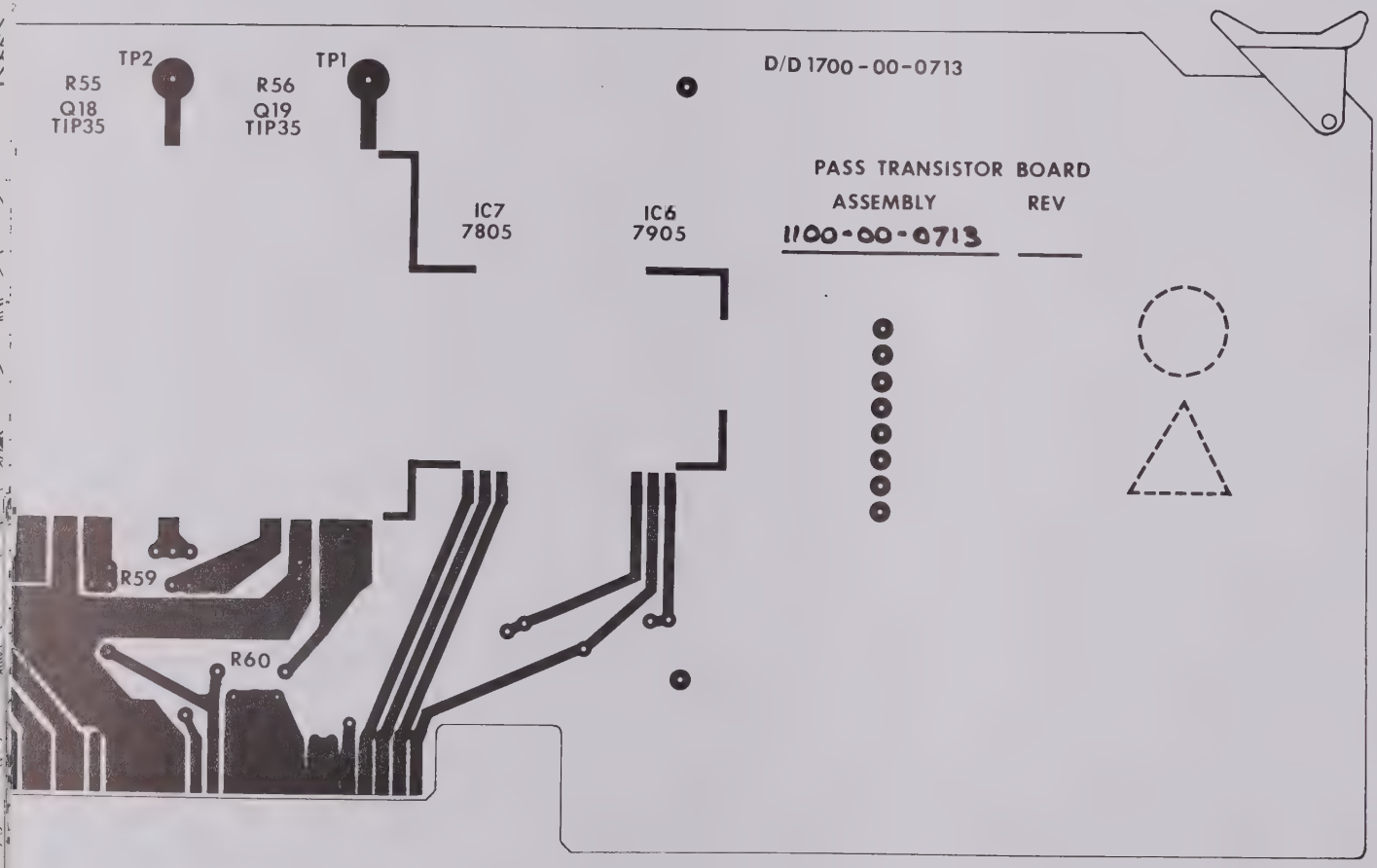


3. I_L (+5V) $\cong$ (V_{TP1} - V_{TP2}) x 20 AMPS .
2. THIS SCHEMATIC IS REFERENCED ON TA
1. ALL I/O PIN DESIGNATIONS ARE ON J14

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN T. FOSTER	DATE 7-1-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Saliga	7 SEPT '77	TITLE SCHEMATIC- PASS TRANSISTOR/REGULATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		MODEL NO.
	DO NOT SCALE DWG		DWG NO. 0103-00-0713 REV C
	SCALE		CODE IDENT 23338 SHEET 1 OF 1

0103-00-0713



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PASS TRANSISTOR PCA
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010 ANGLES ± 1; XX ± .030		MODEL NO: 1720
	DO NOT SCALE DWG		DWG NO: 0101-00-0713
	SCALE		REV
			CODE IDENT: 23338
			SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
ASSY DRWG, REGULATOR	0101-00-0713	WVTK	0101-00-0713	1
SCHEMATIC, REGULATOR	0103-00-0713	WVTK	0103-00-0713	1
HEATSINK REF: 3200-06-0010	1400-00-7933	WVTK	1400-00-7933	1
REGULATOR BD	1700-00-0713	WVTK	1700-00-0713	1
RIGHT ANGLE CONN	87632-8	AMP	2100-02-0078	1
CONNECTOR	JF2P	WINCH	2100-02-0082	1
CABLE CLAMP	832	SMITH	2800-00-0009	1
STANDOFF, SWAGE .125 H, .250 DIA 4-40, .093 MAT'L	6911-2-3C	LYNTR	2800-03-0003	5
PC BD EJECTOR	103 BLACK	CALMK	2800-07-0017	2
WASHER	B51547F015	MOT	2800-11-0015	10
LABLE, CAUTION	B500-B513472-1	BRADY	2800-29-0001	1
INSULATOR, MICA	64-21-023-106	ASHVL	3100-00-0006	7
MICA INSULATOR	10-21-023-212	TI	3100-00-0013	2
RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	2
RES, WW, 10W, 3%, .1 OHM	RH10-.1 OHM 3%	DALE	4702-77-0019	2
TRANS	TIP-29	TI	4902-00-0290	3

GULATOR	ASSEMBLY NO. 1100-00-0713 PAGE: 1	REV E

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TRANS	TIP-30	TI	4902-00-0300	2
TRANS	TIP-35	TI	4902-00-0350	2
THERMOSTAT (185*F)	3001-24-43/B-209	ELMWD	5100-00-0006	1
IC	MC7812CT	MOT	7000-78-1200	1
IC	MC7905CP	MOT	7000-79-0500	1
VOLTAGE REGULATOR	MA7805UC	FAIR	8000-78-0500	1

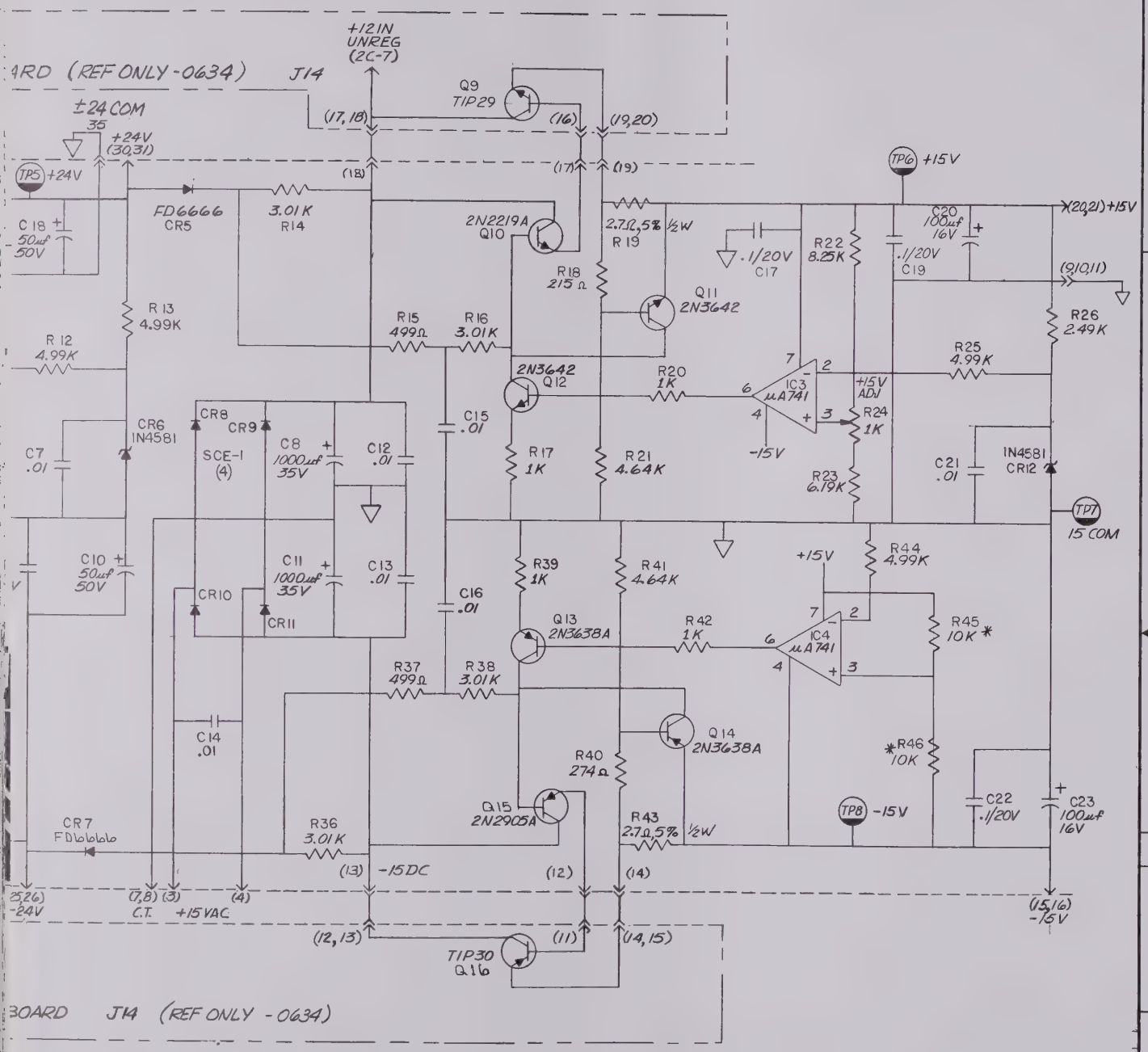
GULATOR	ASSEMBLY NO. 1100-00-0713 PAGE. 2	REV E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, REGULATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ·010 ANGLES ·1 XX ·030		
	DO NOT SCALE DWG	MODEL NO 172B	DWG NO 1100-00-0713 REV E
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

B-SHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894

REV	ECN	BY	DATE	APP
A	ENG IMPRV	TLF	8/2677	
B	ECN 1692, 1687	RO	3-13-78	
C	# 1908 Letterwich		2-6-79	



LAST REF DES USED

C41
CR16
R62
IC8
Q19
TP16

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 6-9-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Sailor	SEPT 7'77	TITLE SCHEMATIC - POWER SUPPLY REGULATOR
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		MODEL NO.
	DO NOT SCALE DWG		DWG NO. 0103-00-0712 REV C
	SCALE		CODE IDENT 23338 SHEET 1 OF 2

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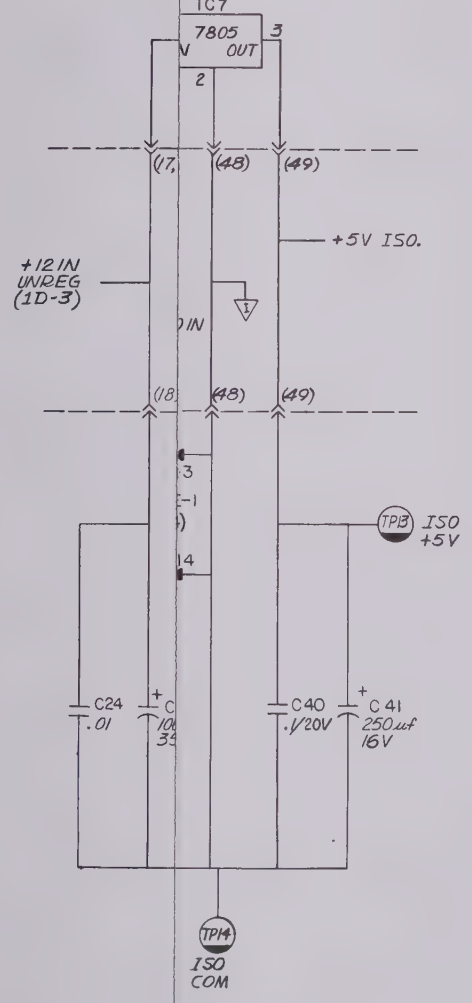
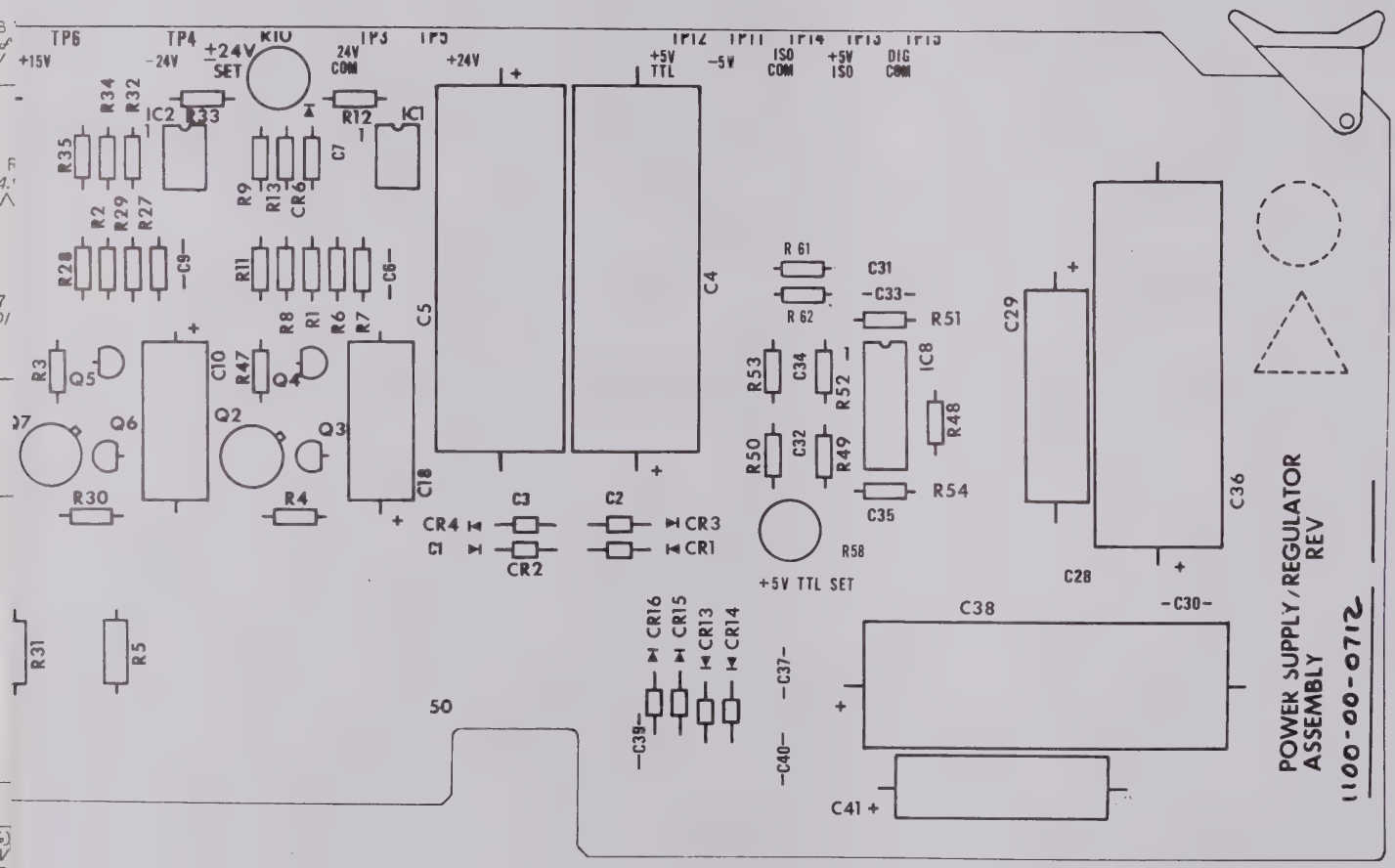
REV	ECN	BY	DATE	APP



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 6-9-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL —	PROJ ENGR & P Tom Saliga	SEPT 7'77	TITLE SCHEMATIC, - POWER SUPPLY REGULATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO.	DWG NO. 0103-00-0712 REV C
	SCALE —	CODE IDENT 23338	SHEET 2 OF 2

NOTE: UNLESS OTHERWISE SPECIFIED



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PWR SUPPLY REGULATOR PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 1728 — DWG NO 0101-00-0712 — REV
	SCALE		CODE IDENT 23338 — SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	2
RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	5
RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	2
RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
RES, SET, 2-10K, 1/8W QTY: 2: 4701-03-1002	142-501-64A	WVTK	4789-00-0019	1
DIODE	1N4581	MICRO	4801-01-4581	2
DIODE	1N4002	FAIR	4801-02-0001	12
DIODE	1N4148	FAIR	4807-02-6666	2
TRANS	2N2219A	NSC	4901-02-2191	2
TRANS	2N2905A	NSC	4901-02-9051	2
TRANS	2N3638A	CARTR	4901-03-6381	2
TRANS	2N3642	FAIR	4901-03-6420	4
TRANS	2N4248	FAIR	4901-04-2480	2
IC	LM741CN	NSC	7000-07-4100	4

ER SUPPLY	ASSEMBLY NO. 1100-00-0712	REV C
	PAGE: 3	

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC	MC1723CP	MOT	7000-17-2300	1

WER SUPPLY	ASSEMBLY NO. 1100-00-0712	REV C
	PAGE: 4	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 XX ±.030	
NOTE UNLESS OTHERWISE SPECIFIED	DO NOT SCALE DWG	
	SCALE	

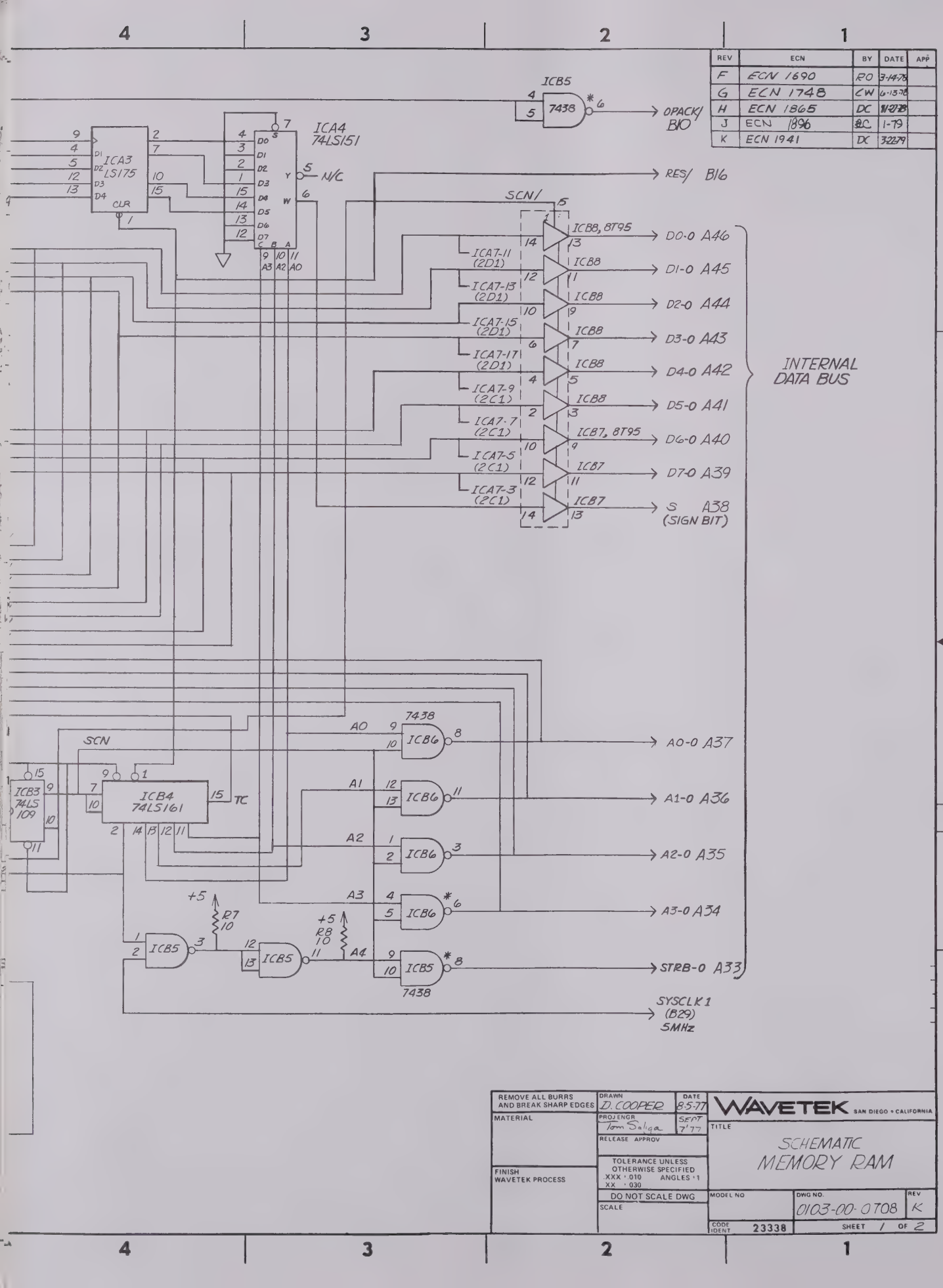
WAVETEK SAN DIEGO • CALIFORNIA

TITLE

PARTS LIST
PCA, POWER SUPPLY

MODEL NO	DWG NO	REV
172B	1100-00-0712	C
CODE IDENT 23338	SHEET 1 OF 1	

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A 3894


4
3
2
1
REV | ECN | BY | DATE | APP
F | ECN 1690 | RO | 3-14-78
G | ECN 1748 | CW | 6-13-78
H | ECN 1865 | DC | 11-27-78
J | ECN 1896 | DC | 1-79
K | ECN 1941 | DC | 32279
ICB5
7438
OPACK/ B10
ICA4 74LS151
ICA3 LS175
CLR
N/C
RES/ B16
SCN/
ICB8, 8T95
ICB7, 8T95
ICB8
ICB7
ICA7-11 (2D1)
ICA7-13 (2D1)
ICA7-15 (2D1)
ICA7-17 (2D1)
ICA7-9 (2C1)
ICA7-7 (2C1)
ICA7-5 (2C1)
ICA7-3 (2C1)
D0-0 A46
D1-0 A45
D2-0 A44
D3-0 A43
D4-0 A42
D5-0 A41
D6-0 A40
D7-0 A39
S A38 (SIGN BIT)
INTERNAL DATA BUS
SCN
ICB3 74LS 109
ICB4 74LS161
TC
A0
A1
A2
A3
A4
ICB6
A0-0 A37
A1-0 A36
A2-0 A35
A3-0 A34
+5
R7 10
R8 10
ICB5
STRB-0 A33
SYSCLK 1 (B29) 5MHz
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER 8-5-77
PROJ ENGR Tom Saliga SENT 7'77
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC MEMORY RAM
MODEL NO
DWG NO. 0103-00-0708
REV K
CODE IDENT 23338
SHEET 1 OF 2

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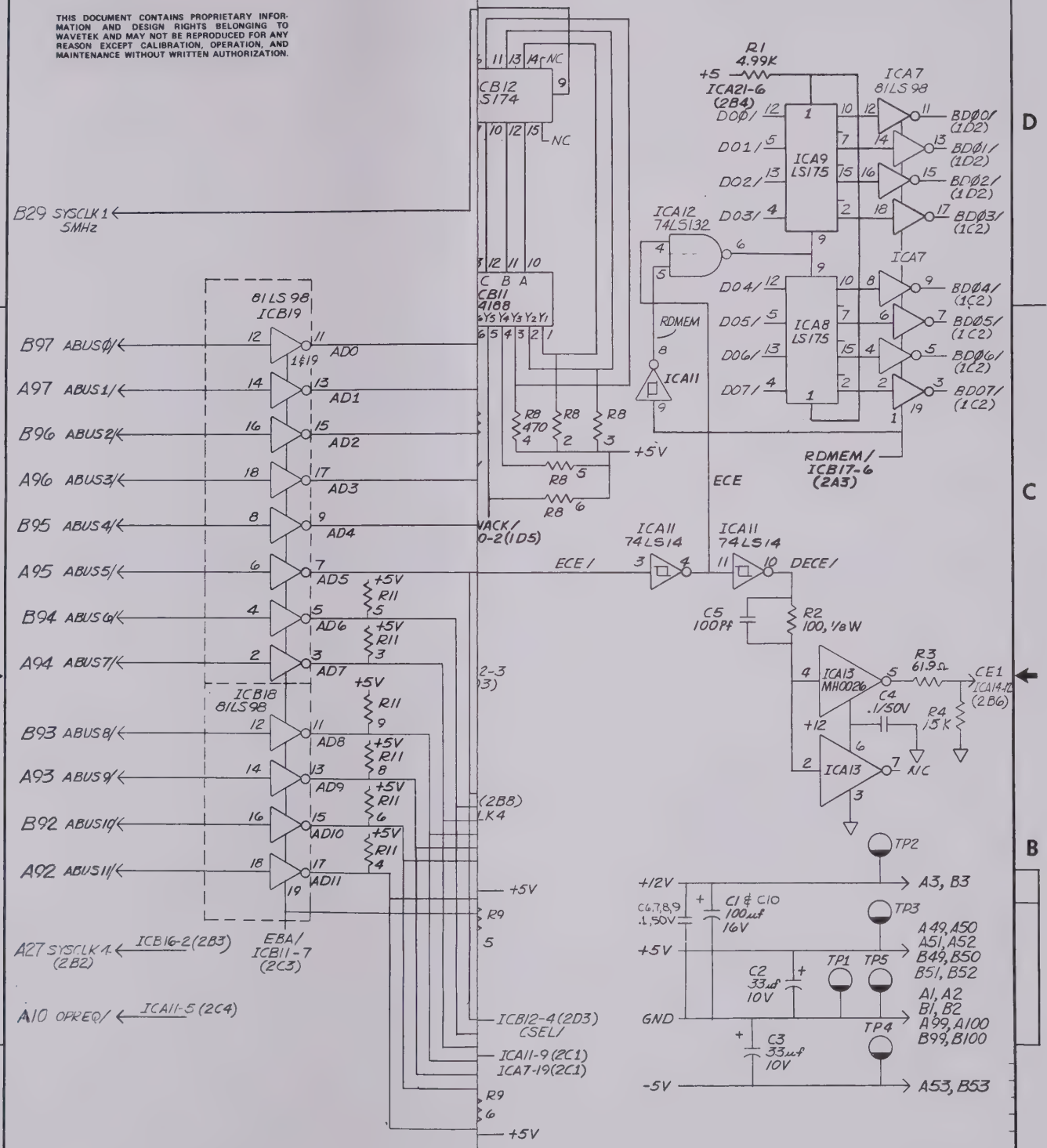
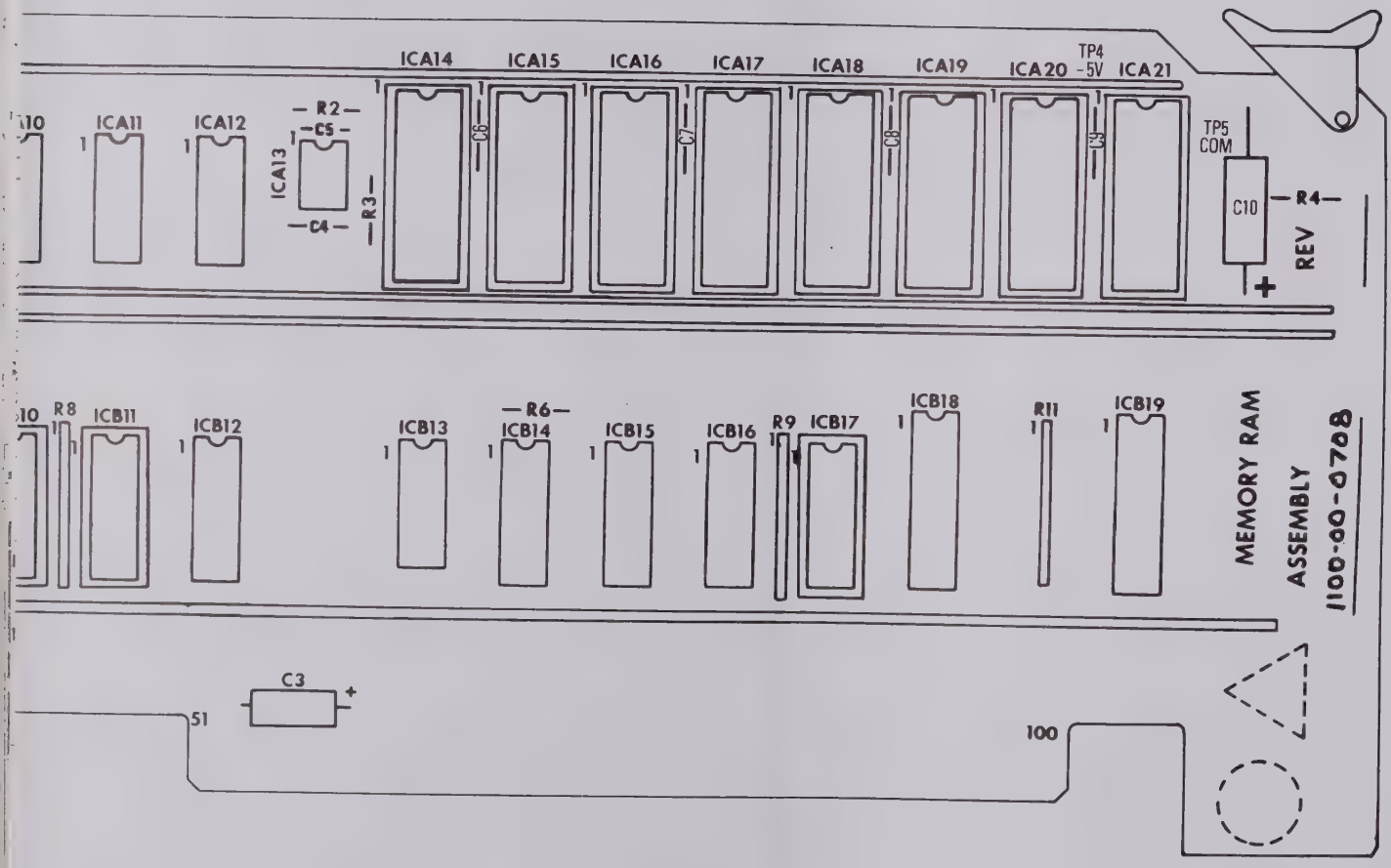
REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 8-5-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Salga	SEPT 7'77	TITLE SCHEMATIC MEMORY RAM
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO
	SCALE		DWG NO 0103-00-0T08 REV K
			CODE IDENT 23338 SHEET 2 OF 2



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: MEMORY RAM PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX · 010 ANGLES · 1 XX · 030		
	DO NOT SCALE DWG		MODEL NO 172 B / DWG NO 0101-00-0708 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

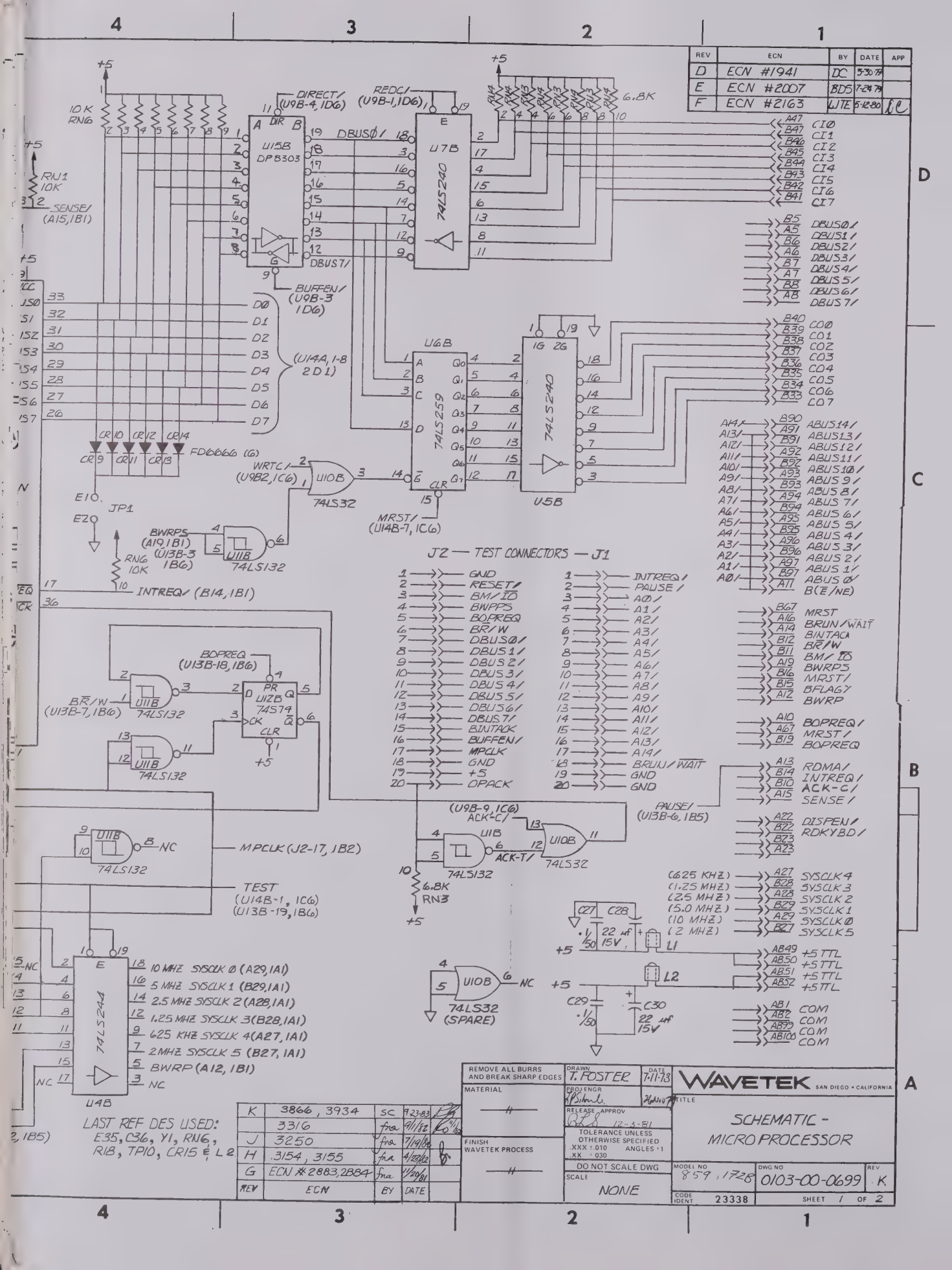
PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC	N74S189A	SIG	8007-41-8900	2
IC, PROGRAMMED REF 8007-41-8801	8600-00-0003	WVTK	8600-00-0003	1
IC, PROGRAMMED REF: 8007-41-8801	8600-00-0004	WVTK	8600-00-0004	1
IC, PROGRAMMED REF 8007-41-8801	8600-00-0169	WVTK	8600-00-0169	1

MEMORY RAM	ASSEMBLY NO 1100-00-0708 PAGE 3	REV J

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE
	RELEASE APPROV		PARTS LIST PCA, MEMORY RAM
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1 XX ± 030		
	DO NOT SCALE DWG	MODEL NO 172B	DWG NO 1100-00-0708 REV J
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A 3994


4
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REV | ECN | BY | DATE | APP
D | ECN #1941 | DC | 5-30-79
E | ECN #2007 | BDS | 7-24-79
F | ECN #2163 | WJTE | 5-12-80
10K RNG
RN1 10K
SENSE/ (A15,1B1)
DIRECT/ (U9B-4,1D6)
REDC/ (U9B-1,1D6)
6.8K
U15B DP8303
U7B 74LS240
DBUS0/
DBUS7/
BUFFEN/ (U9B-3 1D6)
(U14A,1-8 2D1)
D0
D1
D2
D3
D4
D5
D6
D7
CR10 CR12 CR14
CR9 CR11 CR13
FD6666 (6)
E10
E20
JP1
RNG 10K
INTREQ/ (B14,1B1)
U6B 74LS259
U5B 74LS240
WRTC/ (U9B2,1C6)
U11B 74LS32
MRST/ (U14B-7, 1C6)
BWRPS (A19,1B1) (U13B-3 1B6)
U11B 74LS132
J2 — TEST CONNECTORS — J1
GND
RESET/
BM/IO
BWPPS
BOPREQ
BR/W
DBUS0/
DBUS1/
DBUS2/
DBUS3/
DBUS4/
DBUS5/
DBUS6/
DBUS7/
BINTACK
BUFFEN/
MPCLK
GND
+5
OPACK
INTREQ/
PAUSE/
A0/
A1/
A2/
A3/
A4/
A5/
A6/
A7/
A8/
A9/
A10/
A11/
A12/
A13/
A14/
BRUN/WAIT
GND
GND
BOPREQ (U13B-18,1B6)
BR/W (U13B-7,1B6)
U11D 74S74
CLR
MPCLK (J2-17, 1B2)
TEST (U14B-1, 1C6) (U13B-19,1B6)
(U9B-9,1C6) ACK-C/
ACK-T/
U10B 74LS32
6.8K RN3
PAUSE/ (U13B-6, 1B5)
U4B 74LS244
10 MHZ SYSCLK 0 (A29,1A1)
5 MHZ SYSCLK 1 (B29,1A1)
2.5 MHZ SYSCLK 2 (A28,1A1)
1.25 MHZ SYSCLK 3 (B28,1A1)
625 KHZ SYSCLK 4 (A27,1A1)
2 MHZ SYSCLK 5 (B27,1A1)
BWRP (A12, 1B1)
NC
LAST REF DES USED: E35, C36, Y1, RN6, R18, TP10, CR15 & L2
U10B 74LS32 (SPARE)
C27 .1/50
C28 22 uf 15V
L1
L2
C29 .1/50
C30 22 uf 15V
(.625 KHZ) SYSCLK 4
(1.25 MHZ) SYSCLK 3
(2.5 MHZ) SYSCLK 2
(5.0 MHZ) SYSCLK 1
(10 MHZ) SYSCLK 0
(2 MHZ) SYSCLK 5
+5 TTL
COM
ABUS14/
ABUS13/
ABUS12/
ABUS11/
ABUS10/
ABUS 9/
ABUS 8/
ABUS 7/
ABUS 6/
ABUS 5/
ABUS 4/
ABUS 3/
ABUS 2/
ABUS 1/
ABUS 0/
B(E/NE)
MRST
BRUN/WAIT
BINTACK
BR/W
BM/IO
BWRPS
MRST/
BFLAG/
BWRP
BOPREQ/
MRST/
BOPREQ
RDMA/
INTREQ/
ACK-C/
SENSE/
DISPEN/
RDKYBD/
K 3866, 3934 SC 9-23-83
J 3316 fna 9/11/82
H 3250 fna 7/19/82
G 3154, 3155 fna 4/20/82
F ECN #2883,2884 fna 1/20/81
REV | ECN | BY | DATE
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN T. FOSTER 7-11-78
PROJ ENGR
RELEASE APPROV 12-3-81
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 XX .030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC - MICRO PROCESSOR
MODEL NO 859, 1728
DWG NO 0103-00-0699
REV K
CODE IDENT 23338
SHEET 1 OF 2

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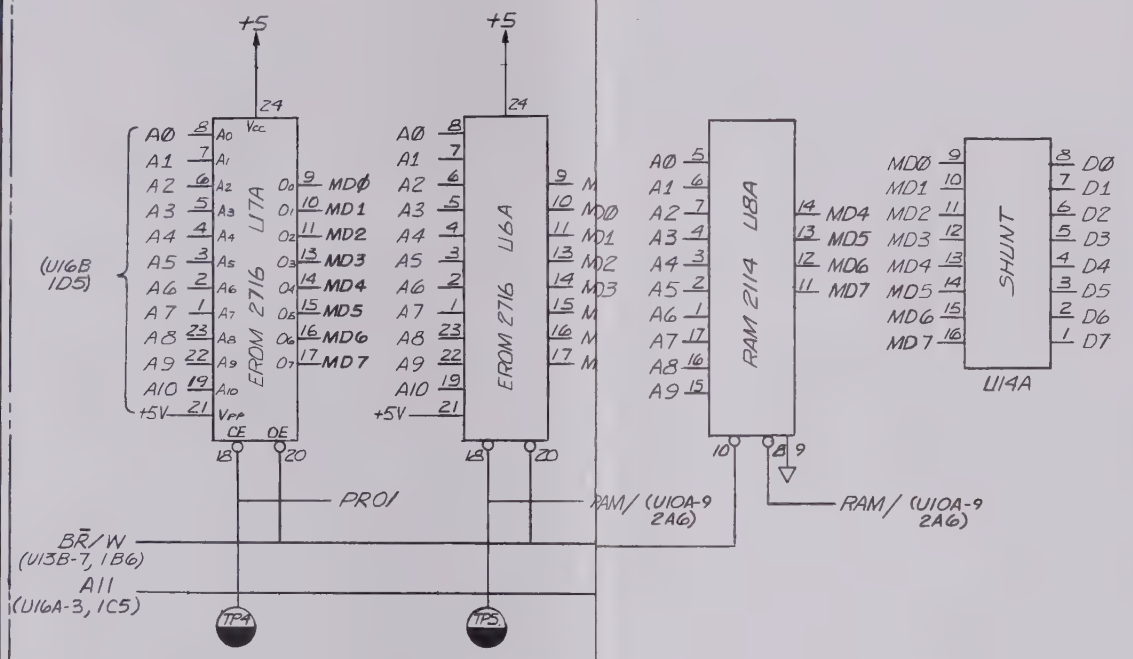
REV	ECN	BY	DATE	APP

NOT

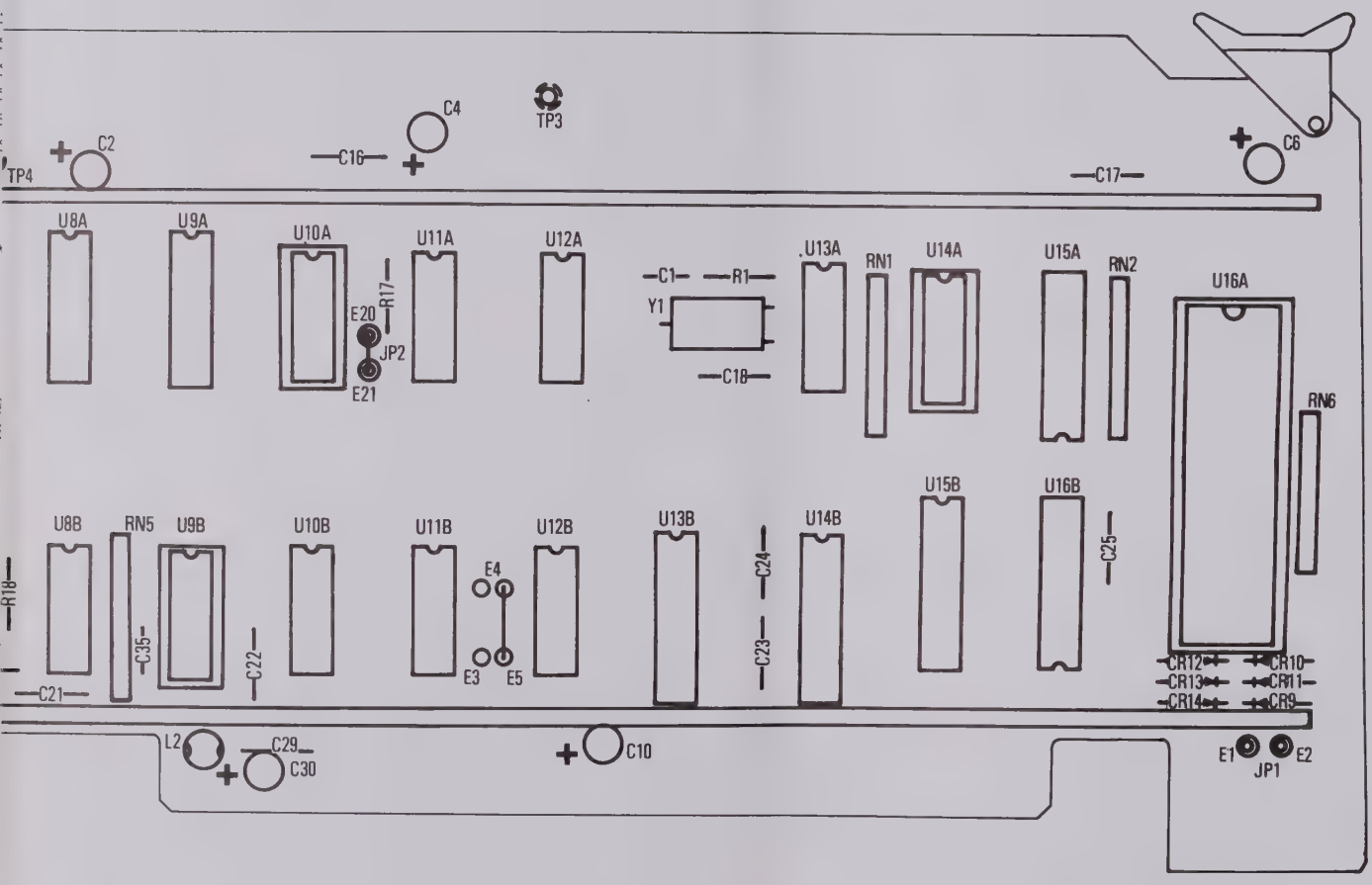


(U13B-5, 1B6) BM/IO
(U13B-18, 1B6) BOPREQ
(U13A-8, 1C7) INTACK/

(U15A
U15A-5
(U14B-12
(U14B-14

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN T. FOSTER	DATE 7-12-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
	RELEASE APPROV		SCHEMATIC - MICROPROCESSOR (EPROM MEMORY)
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO	DWG NO 0103-00-0699 REV K
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: MICROPROCESSOR PCA
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010 ANGLES ± 1; XX ± .030		
	DO NOT SCALE DWG		MODEL NO: 172B; DWG NO: 0101-00-0699; REV
	SCALE		CODE IDENT: 23338; SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TRANSIPAD	10123N	METRS	2800-11-0003	2
SHUNT	435704-8	AMP	3000-00-0033	1
JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	1
PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	4
BALUN CORE	2873000902	FARIT	3100-00-0002	2
RES, MF, 1/8W, 1%, 11K	RN55D-1102F	TRW	4701-03-1102	1
RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	8
RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	3
RES NETWK	785-1R1.5K	BECK	4770-00-0010	1
RES MODULE	4310R-101-682	BOURN	4770-00-0016	2
DIODE	1N34	FAIR	4804-01-0034	1
DIODE	1N4148	FAIR	4807-02-6666	7
POWER BUSS BAR (LG)	6009-90-0004	WVTK	6009-90-0004	2
IC	2114	INTEL	8000-21-1400	2

-PROC	ASSEMBLY NO. 1100-00-0699 PAGE: 2	REV H

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC	SCN2650AC2N40	SIG	8000-26-5001	1
IC	7404	TI	8000-74-0400	1
IC	SN74LS13N	TI	8000-74-1310	1
IC	74LS32	TI	8000-74-3210	1
IC	74LS38	TI	8000-74-3810	1
IC	74S74	TI	8000-74-7401	1
IC	DP8303	NAT	8000-83-0300	3
IC	74LS132	TI	8007-41-3210	2
IC	74LS161	SIG	8007-41-6110	1
IC	74LS192	TI	8007-41-9210	2
IC	74LS240	TI	8007-42-4010	3
IC	74LS244	TI	8007-42-4410	2
IC	SN74LS259N	TI	8007-42-5910	1
IC, PROGRAMMED REF 8007-41-8801	8600-00-0193	WVTK	8600-00-0193	1
IC, PROGRAMMED REF 8007-41-8801	8600-00-0194	WVTK	8600-00-0194	1
IC PROGRAMMED FROM 8000-27-3200	8600-00-0227	WVTK	8600-00-0227	1

-PROC	ASSEMBLY NO. 1100-00-0699 PAGE 3	REV H

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN | DATE

PROJ ENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

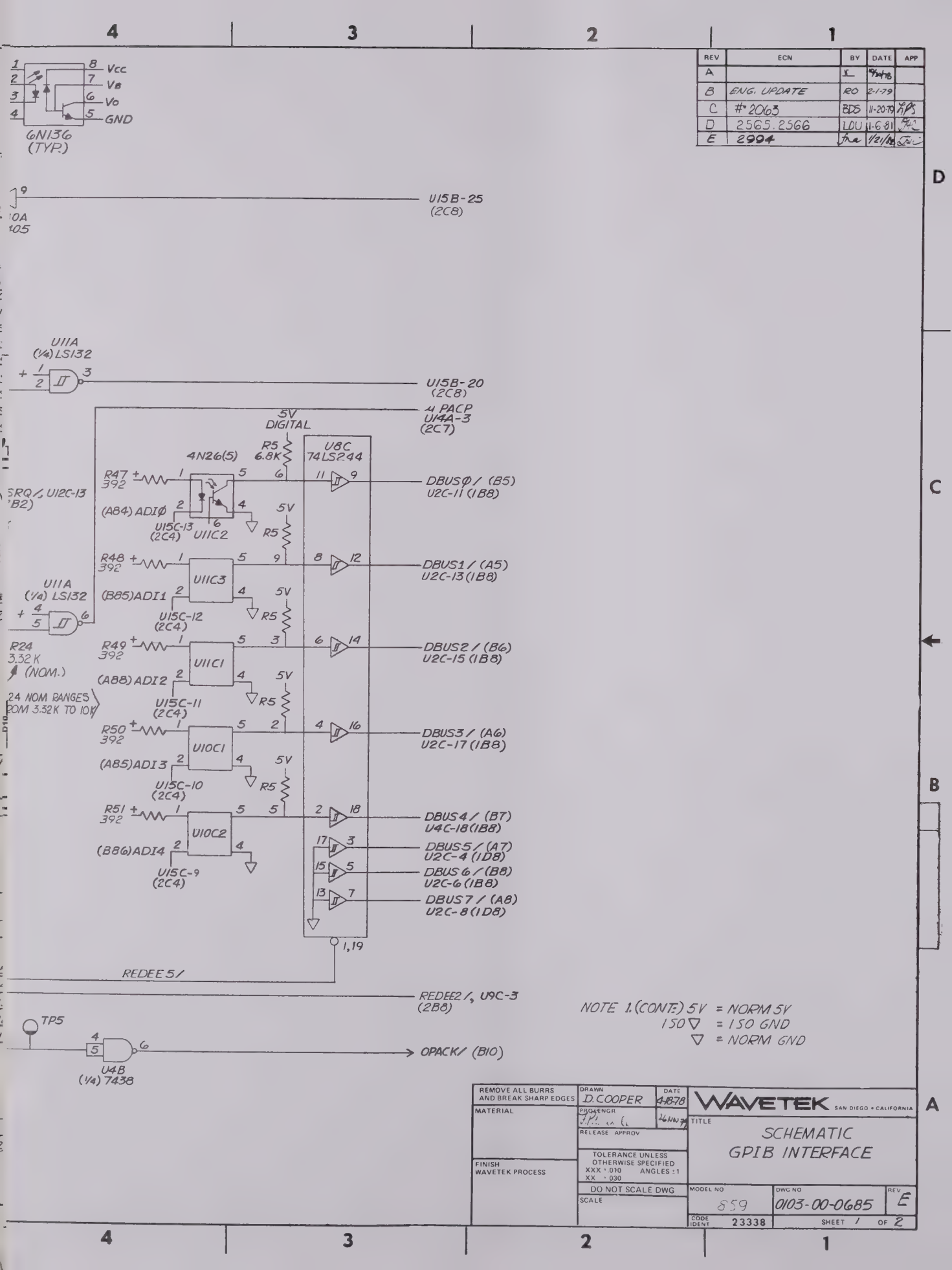
PARTS LIST
PCA, M-PROC

MODEL NO	DWG NO	REV
172B	1100-00-0699	H

CODE IDENT 23338 SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894


4
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1
REV | ECN | BY | DATE | APP
A | | | |
B | ENG. UPDATE | RO | 2-1-79 |
C | #2063 | BDS | 11-20-79 |
D | 2565.2566 | LDU | 11-6-81 |
E | 2994 | | 1/21/82 |
D
C
B
A
6N136 (TYP.)
Vcc
VB
Vo
GND
U15B-25 (2C8)
U11A (1/4) LS132
U15B-20 (2C8)
4 PACP U14A-3 (2C7)
5V DIGITAL
4N26(5)
R5 6.8K
U8C 74LS244
R47 392
R48 392
R49 392
R50 392
R51 392
U11C3
U11C1
U10C1
U10C2
(A84) ADIØ
(B85)ADI1
(A88) ADI2
(A85)ADI3
(B86)ADI4
U15C-13 (2C4)
U15C-12 (2C4)
U15C-11 (2C4)
U15C-10 (2C4)
U15C-9 (2C4)
DBUSØ/ (B5) U2C-11 (1B8)
DBUS1/ (A5) U2C-13 (1B8)
DBUS2/ (B6) U2C-15 (1B8)
DBUS3/ (A6) U2C-17 (1B8)
DBUS4/ (B7) U4C-18 (1B8)
DBUS5/ (A7) U2C-4 (1D8)
DBUS6/ (B8) U2C-6 (1B8)
DBUS7/ (A8) U2C-8 (1D8)
1,19
REDEE5/
REDEE2/, U9C-3 (2B8)
R24 3.32K (NOM.)
24 NOM RANGES FROM 3.32K TO 10K
TP5
U4B (1/4) 7438
OPACK/ (B10)
NOTE 1. (CONT.) 5V = NORM 5V
150 ▽ = 150 GND
▽ = NORM GND
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER 4-18-78
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC GPIB INTERFACE
MODEL NO 859
DWG NO 0103-00-0685
REV E
CODE IDENT 23338
SHEET 1 OF 2

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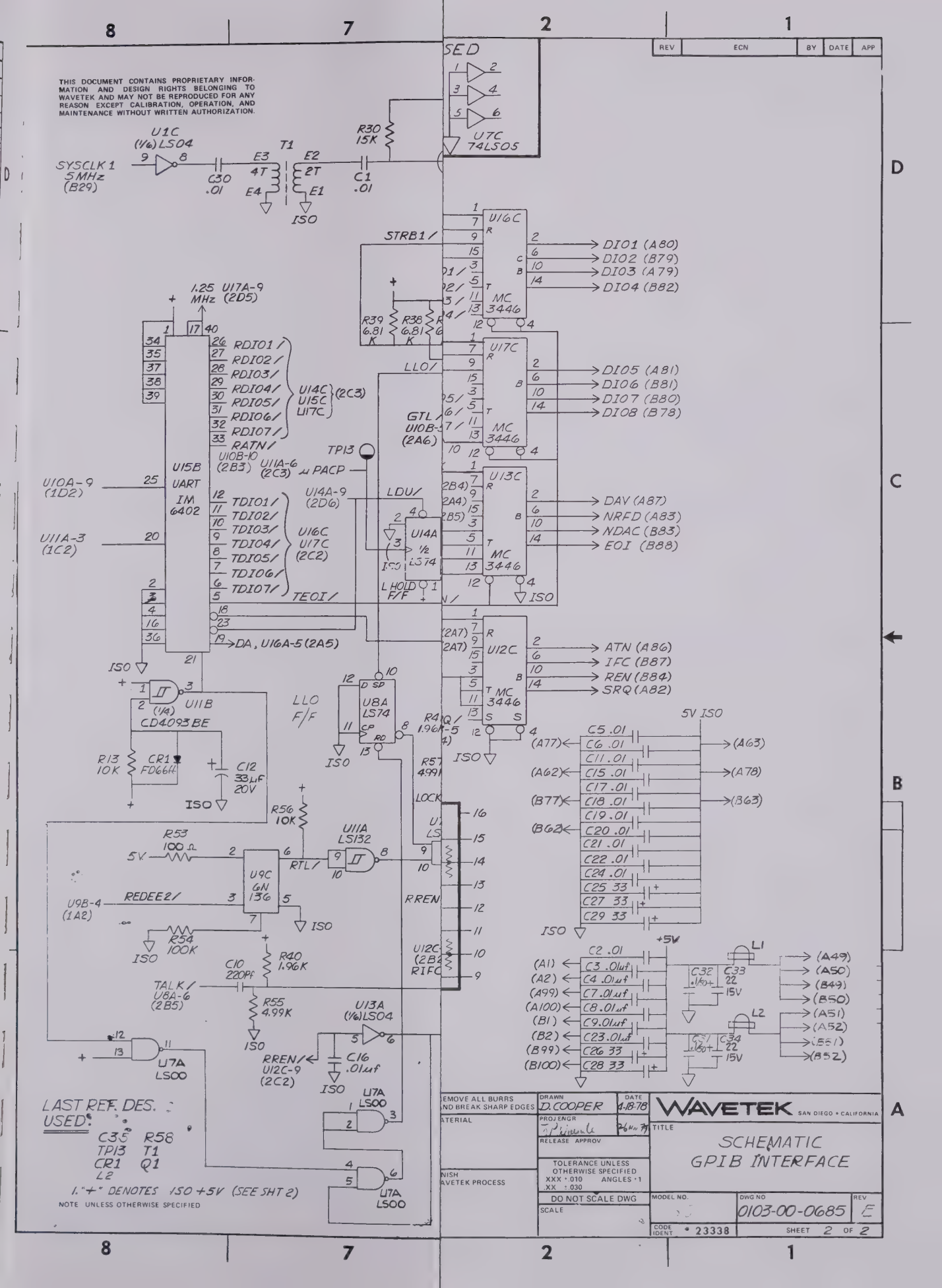
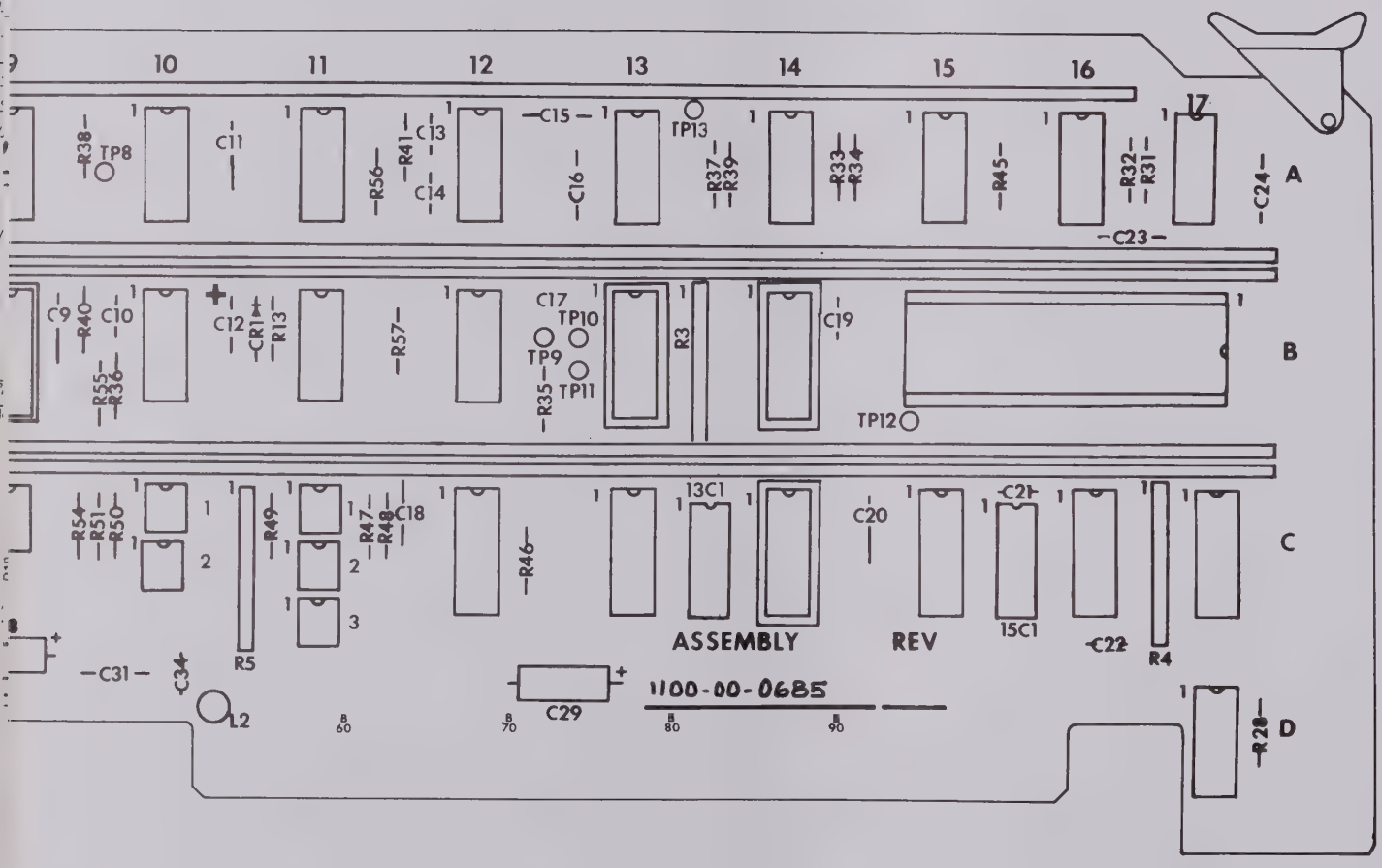
REV	ECN	BY	DATE	APP



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 4-18-78	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
FINISH WAVETEK PROCESS	RELEASE APPROV		SCHEMATIC GPIB INTERFACE
DO NOT SCALE DWG	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	MODEL NO.	DWG NO 0103-00-0685 REV E
	SCALE	CODE IDENT • 23338	SHEET 2 OF 2



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: GPIB INTERFACE PCA
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010 ANGLES ± 1; XX ± .030		
	DO NOT SCALE DWG		MODEL NO: 172B; DWG NO: 0101-00-0685; REV:
	SCALE		CODE IDENT: 23338; SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
DIODE	1N4148	FAIR	4807-02-6666	1
TRANS	2N3903	NSC	4901-03-9030	1
POWER BUSS BAR (LG)	6009-90-0004	WVTK	6009-90-0004	4
POWER BUSS BAR (ST)	6009-90-0005	WVTK	6009-90-0005	1
OPTO-COUPLER	4N26	MOT	7000-04-2600	8
IC	6N136	SPECT	7100-00-0001	7
IC	MC3446P	MOT	8000-34-4600	4
IC	CD4093BE	RCA	8000-40-9300	1
IC	IM6402CPL	INTSL	8000-64-0200	2
IC	74LS00	TI	8000-74-0010	2
IC	74LS04	TI	8000-74-0410	2
IC	7405	TI	8000-74-0500	1
IC	74LS05	TI	8000-74-0510	3
IC	74LS08	TI	8000-74-0810	1
IC	74LS11	TI	8000-74-1110	1
IC	74LS32	TI	8000-74-3210	1

GPIB INTERFACE | ASSEMBLY NO. 1100-00-0685 | PAGE: 3 | REV D

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC	7438	TI	8000-74-3800	1
IC	74LS74	TI	8000-74-7410	8
IC	93L24PC	FAIR	8000-93-2410	1
IC	MC14006BCP	MOT	8001-40-0600	1
IC	74LS132	TI	8007-41-3210	2
IC	74LS240	TI	8007-42-4010	2
IC	74LS244	TI	8007-42-4410	2
IC, PROGRAMMED REF: 8007-41-8801	8600-00-0092	WVTK	8600-00-0092	1
IC, PROGRAMMED REF: 8007-41-8801	8600-00-0163	WVTK	8600-00-0163	1
IC, PROGRAMMED REF: 8007-41-8801	8600-00-0164	WVTK	8600-00-0164	1
IC, PROGRAMMED REF: 8008-21-2601	8600-00-0165	WVTK	8600-00-0165	1

GPIB INTERFACE | ASSEMBLY NO. 1100-00-0685 | PAGE: 4 | REV D

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE

MATERIAL | PROJ ENGR

RELEASE APPROV

FINISH WAVETEK PROCESS

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

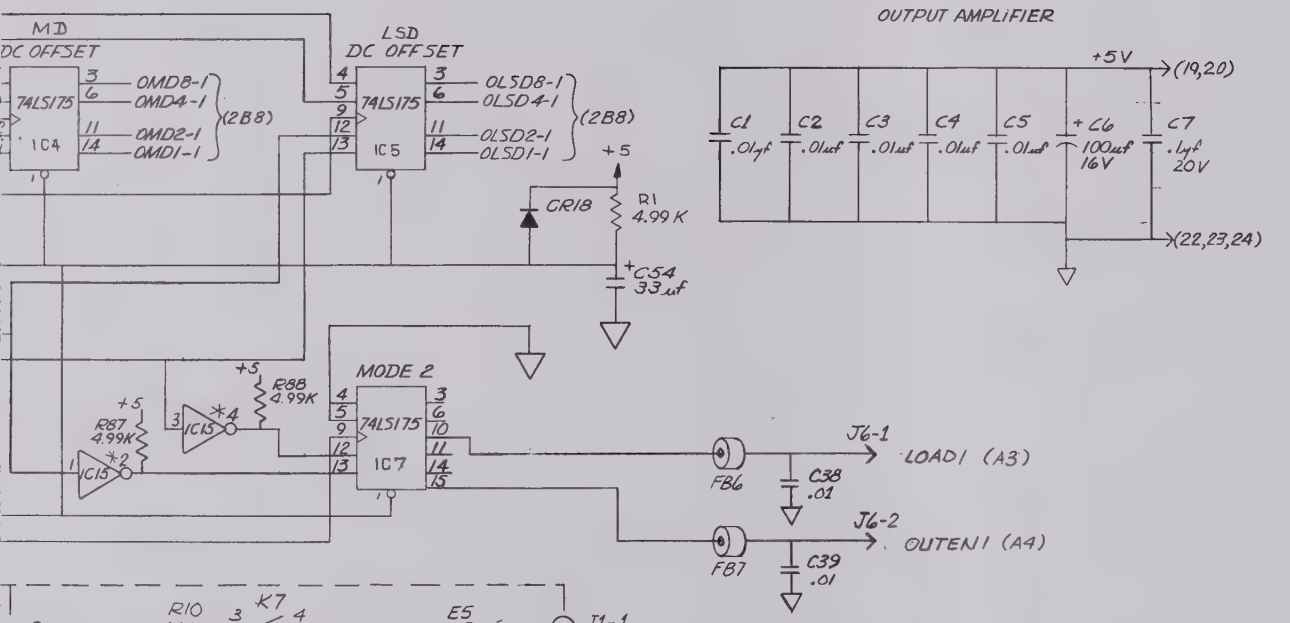
PARTS LIST
PCA, GPIB INTERFACE

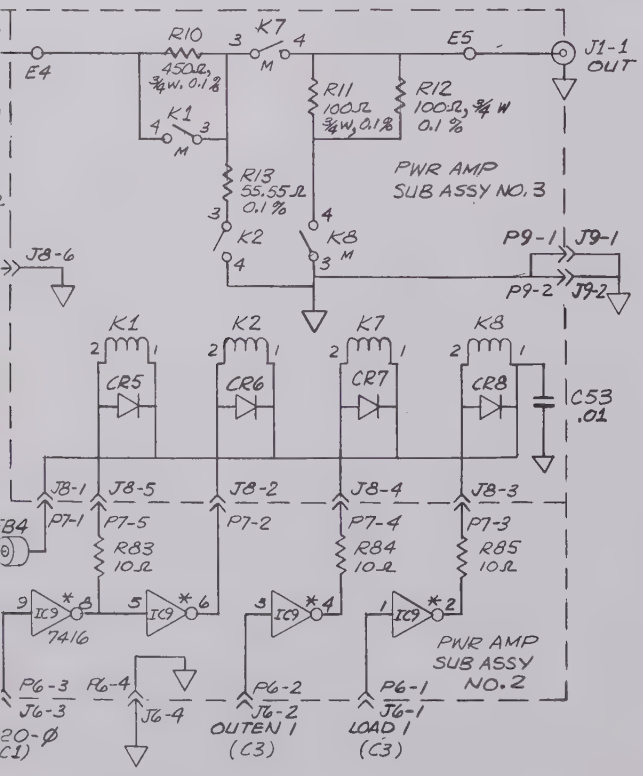
MODEL NO	DWG NO	REV
172B	1100-00-0685	D

CODE IDENT 23338 | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894

REV	ECN	BY	DATE	APP
A	ADD R86	TLF	6/6/77	
B	ENG. IMPRVMT			
C	ECN 1707	RO	4-17-78	
D	ECN 1843	BDS	11-11-78	





REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN T. FOSTER	DATE 3-29-77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Sabyan	SEPT 0 '77	TITLE SCHEMATIC POWER AMPLIFIER/ DC OFFSET
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO.	DWG NO. 0103-00-0710 REV D
	SCALE	CODE IDENT 23338	SHEET 1 OF 2

0103-00-0710

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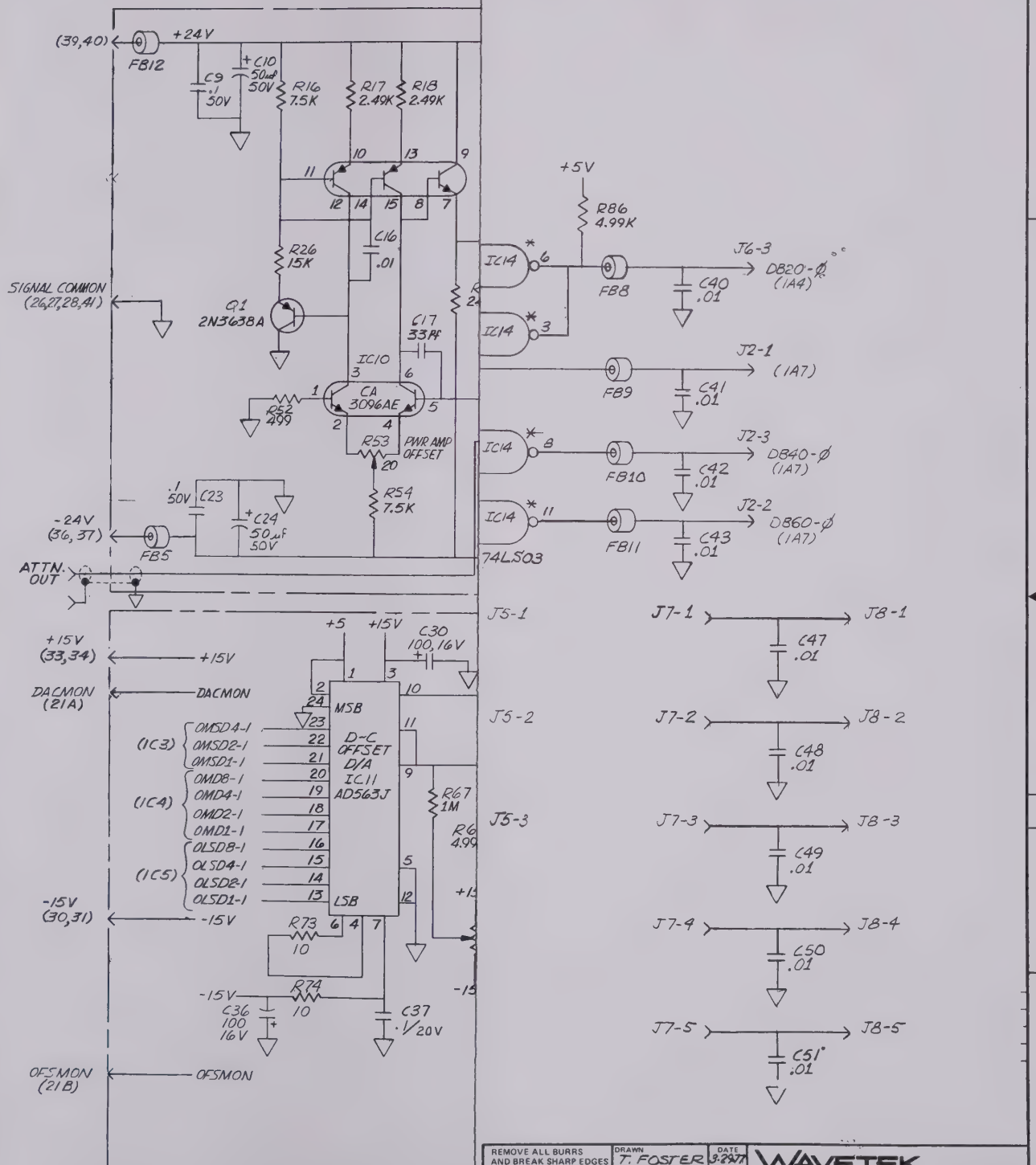
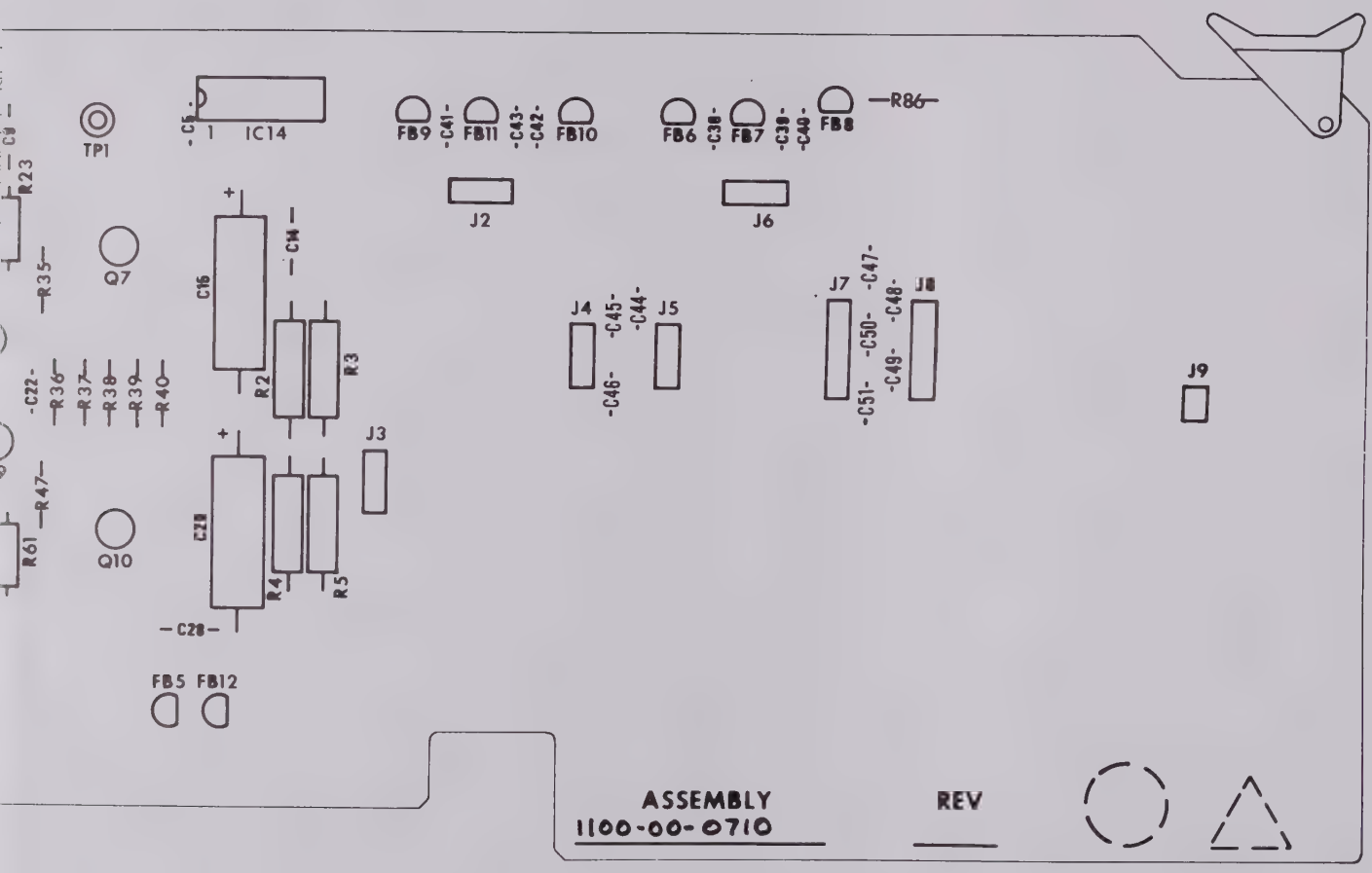
REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS IN OHMS 1/8W
2. ALL CAPACITORS IN MICROFAR
3. □ = 0.1% 1/8W RES.
4. Δ MATCHED SET = 4789-
5. ALL UNMARKED DIODES - FD

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN T. FOSTER	DATE 9.29.77	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROLENGR Tom Saliga	SEPT 8'77	TITLE SCHEMATIC POWER AMPLIFIER DC OFFSET
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO	DWG NO 0103-00-0710 REV A
	SCALE	CODE IDENT 23338	SHEET 2 OF 2



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: POWER AMPLIFIER PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 172B / DWG NO 0101-00-0710 / REV
	DO NOT SCALE DWG		
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, PWR AMPL	0101-00-0710					
NONE	SCHEMATIC, PWR AMPL	0103-00-0710	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	2
1	PWR AMPL SUB ASSY #1	172-591	RES, MF, 1/4W, 1%, 1M	RN60D-1004F	TRW	4701-13-1004	1
2	PWR AMPL SUB ASSY #2	172-592	RES, SET, 2-10K, 1/8W GTY: 2: 4701-03-1002	142-501-64A	WVTK	4789-00-0019	1
3	PWR AMPL SUB ASSY #3	172-593	RES, MF, 3/4W, .1%, 200	ML212-200	CADDO	4799-00-0047	4
NONE	SHIELD, RF	1400-00-7091	DIODE	1N4581	MICRO	4801-01-4581	1
NONE	SHIELD, RF	1400-00-7101	DIODE	1N4148	FAIR	4807-02-6666	9
NONE	SHIELD, RF	1400-00-7111					
NONE	SHIELD, RF	1400-00-7121	TRANS	2N2219A	NSC	4901-02-2191	1
NONE	SHIELD, RF	1400-00-7131	TRANS	2N2905A	NSC	4901-02-9051	2
NONE	COVER, RF SHIELD	1400-00-7143	TRANS	2N3638A	CARTR	4901-03-6381	1
NONE	X, CORNER POST REF: 3200-02-0004	1400-00-7439	TRANS	2N3866	MOT	4901-03-8660	1
NONE	T-CORNER POST REF: 3200-02-0004	1400-00-7449	TRANS	2N3903	NSC	4901-03-9030	1
			TRANS	2N4047	FAIR	4901-04-0470	1
NONE	SHIELD, RF	1400-00-7451	TRANS	2N5139	FAIR	4901-05-1390	2
C21	CAP, CER, 5PF, 1KV	DD-050	TRANS	2N5160-18	MOT	4901-05-1600	1
C20	CAP, CER, 10PF, 1KV	DD-100	TRANS	2N5462	MOT	4901-05-4620	2
C1 C11 C16 C18 C19 C2	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z10	CABLE, COAX, 26AWG	RG 174/U	ITT	6001-40-0001	1

WAVETEK PARTS LIST	TITLE PCA, PWR AMPL	ASSE 110 WR AMPL PAG	ASSEMBLY NO. 1100-00-0710 PAGE: 5	REV D

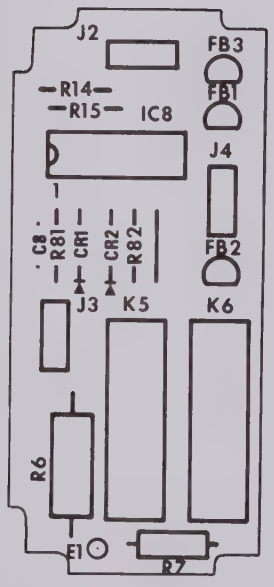
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C22 C25 C26 C3 C31 C34 C35 C38 C39 C4 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C5 C50 C51			IC	AD563J	ANDEV	7000-05-6300	1
			IC	LM741CN	NSC	7000-07-4100	2
C13 C14 C23 C27 C28 C32 C33 C37 C7 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z05	IC	CA-3096AE	RCA	7000-30-9600	1
			IC	74LS03	TI	8000-74-0310	1
C17	CAP, CER, 33PF, 1KV	DD-330	IC	7416	SIG	8000-74-1600	1
C30 C36 C6	CAP, ELECT, 100MF, 16V	500D1070016DC7	IC	74LS139	SIG	8007-41-3910	2
C10 C15 C24 C29	CAP, ELECT, 50MF, 50V	500D5060050DD7	IC	74LS175	TI	8007-41-7510	5
C12	CAP, VAR, 3.5-13PF250V	300422-411					
C54	CAP, TANT, 33MF, 10V	150D336X9010B2					
NONE	PWR AMPL, OFFSET BD	1700-00-0710					
NONE	SKT, IC, 24PIN	DILB-24P-108					
NONE	TERM	2010B1					
TP1 TP2 TP4	CONN	60598-8					
4	CONN PIN, MALE UOM-EA PIN	CAS36SP-100-22					
NONE	CONN	27-843					
J1	CONN	27-3					
4	PC BD EJECTOR	103 GRAY					

WAVETEK PARTS LIST	TITLE PCA. PWR AMPL	ASS 110 WR AMPL PAG	ASSEMBLY NO. 1100-00-0710 PAGE: 6	REV D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST PCA, PWR AMPL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 172B / DWG NO 1100-00-0710 / REV D
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPH.CS/ACCUPRESS REORDER NO A 3894



1208-00-0591

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROTENGR		TITLE ASSEMBLY POWER AMPLIFIER SUB. ASSY. NO. 1
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG		MODEL NO 172 / DWG NO 0101-00-0591 / REV
	SCALE		CODE IDENT 23338 / SHEET OF

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
ASSY DRWG PWR AMPL#1	0101-00-0591	WVTK	0101-00-0591	1
SCHEMATIC, PWR AMPL	0103-00-0710	WVTK	0103-00-0710	1
CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
PWR AMPL BD #1	1700-00-0591	WVTK	1700-00-0591	1
CONN	22-17-2042	MOLEX	2100-02-0065	3
TRANSIPAD	10123N	METRS	2800-11-0003	3
BALUN CORE	2873000902	FARIT	3100-00-0002	3
RELAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	1
RELAY, FORM A MERCURY	4500-00-0012	WVTK	4500-00-0012	1
RES, MF, 1/8W, .1%, 55.5	RN55E55R5B	MEPCO	4701-02-5559	1
RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	2
RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	2
RES, MF, 3/4W, .1%, 450	ML212-450	CADDO	4799-00-0046	1
DIODE	1N4148	FAIR	4807-02-6666	2
WIRE, WIREWRAP 24GA. KYNAR INSULATION	UL1422 W/W WIRE WHT	BRDRX	6000-52-4009	1
IC	7416	SIG	8000-74-1600	1

MPL SUB ASSY #1	ASSEMBLY NO. 1208-00-0591 PAGE: 1	REV C

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN | DATE

PROJ ENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

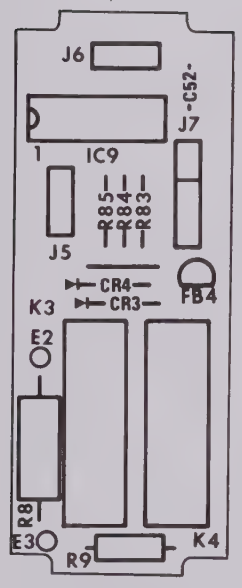
PARTS LIST
PWR AMPL SUB ASSY #1

MODEL NO	DWG NO.	REV
172B	1208-00-0591	C

CODE IDENT 23338 | SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894



1208-00-0592

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY POWER AMPLIFIER SUB. ASSY. NO. 2
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG		MODEL NO 172 / DWG NO 0101-00-0592 / REV
	SCALE		CODE IDENT 23338 / SHEET OF

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REV	ECN	BY	DATE	APP

ART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
SSY DRWG PWR AMPL#2	0101-00-0592	WVTK	0101-00-0592	1
CHEMATIC, PWR AMPL	0103-00-0710	WVTK	0103-00-0710	1
AP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
WR AMPL SUB BD #2	1700-00-0592	WVTK	1700-00-0592	1
ONN	22-17-2022	MOLEX	2100-02-0061	1
ONN	22-17-2042	MOLEX	2100-02-0065	3
PRING SOCKET	50935-1	AMP	2100-03-0039	1
RANSIPAD	10123N	METRS	2800-11-0003	1
ALUN CORE	2873000902	FARIT	3100-00-0002	1
ELAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	1
ELAY, FORM A MERCURY	4500-00-0012	WVTK	4500-00-0012	1
ES, MF, 1/8W, .1%, 55.5	RN55E55R5B	MEPCO	4701-02-5539	1
ES, MF, 1/8W, 1%, 10	RN55D-10ROF	TRW	4701-03-1009	3
ES, MF, 3/4W, .1%, 450	ML212-450	CADDO	4799-00-0046	1
IODE	1N4148	FAIR	4807-02-6666	2
IRE, WIREWRAP 24GA. YNAR INSULATION	UL1422 W/W WIRE WHT	BRDRX	6000-52-4009	1
C	7416	SIG	B000-74-1600	1

L SUB ASSY #2	ASSEMBLY NO. 1208-00-0592	REV D
	PAGE: 1	

EMOVE ALL BURRS
ND BREAK SHARP EDGES
ATERIAL

NISH
AVETEK PROCESS

NOTE UNLESS OTHERWISE SPECIFIED

DRAWN	DATE
PROJ ENGR	
RELEASE APPROV	

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ±1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

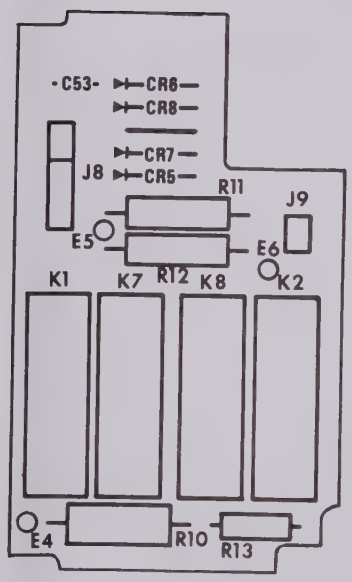
TITLE

PARTS LIST
PWR AMPL SUB ASSY #2

MODEL NO	DWG NO	REV
172B	1208-00-0592	D

CODE IDENT 23338 SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894



1208-00-0593

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY POWER AMPLIFIER SUB ASSY. NO. 3
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX 010 ANGLES 1 XX 030		
	DO NOT SCALE DWG		MODEL NO 172 / DWG NO 0101-00-0593 / REV
	SCALE		CODE IDENT 23338 / SHEET OF

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REV	ECN	BY	DATE	APP

RT DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
SY DRWG PWR AMPL#3	0101-00-0593	WVTK	0101-00-0593	1
HEMATIC, PWR AMPL	0103-00-0710	WVTK	0103-00-0710	1
P, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNO	1500-01-0310	1
R AMPL BD #3	1700-00-0593	WVTK	1700-00-0593	1
NN	22-17-2022	MOLEX	2100-02-0061	2
NN	22-17-2042	MOLEX	2100-02-0063	1
RING SOCKET	50935-1	AMP	2100-03-0039	2
LAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	1
LAY, FORM A MERCURY	4500-00-0012	WVTK	4500-00-0012	3
S, MF, 1/8W, .1%, 55.5	RN55E55R5B	MEPCO	4701-02-5559	1
S, MF, 3/4W, .1%, 100	ML212-100	CADDO	4799-00-0038	2
S, MF, 3/4W, .1%, 450	ML212-450	CADDO	4799-00-0046	1
ODE	1N4148	FAIR	4807-02-6666	4
RE, WIREWRAP 24GA. NAR INSULATION	UL1422 W/W WIRE WHT	BRDRX	6000-52-4009	1

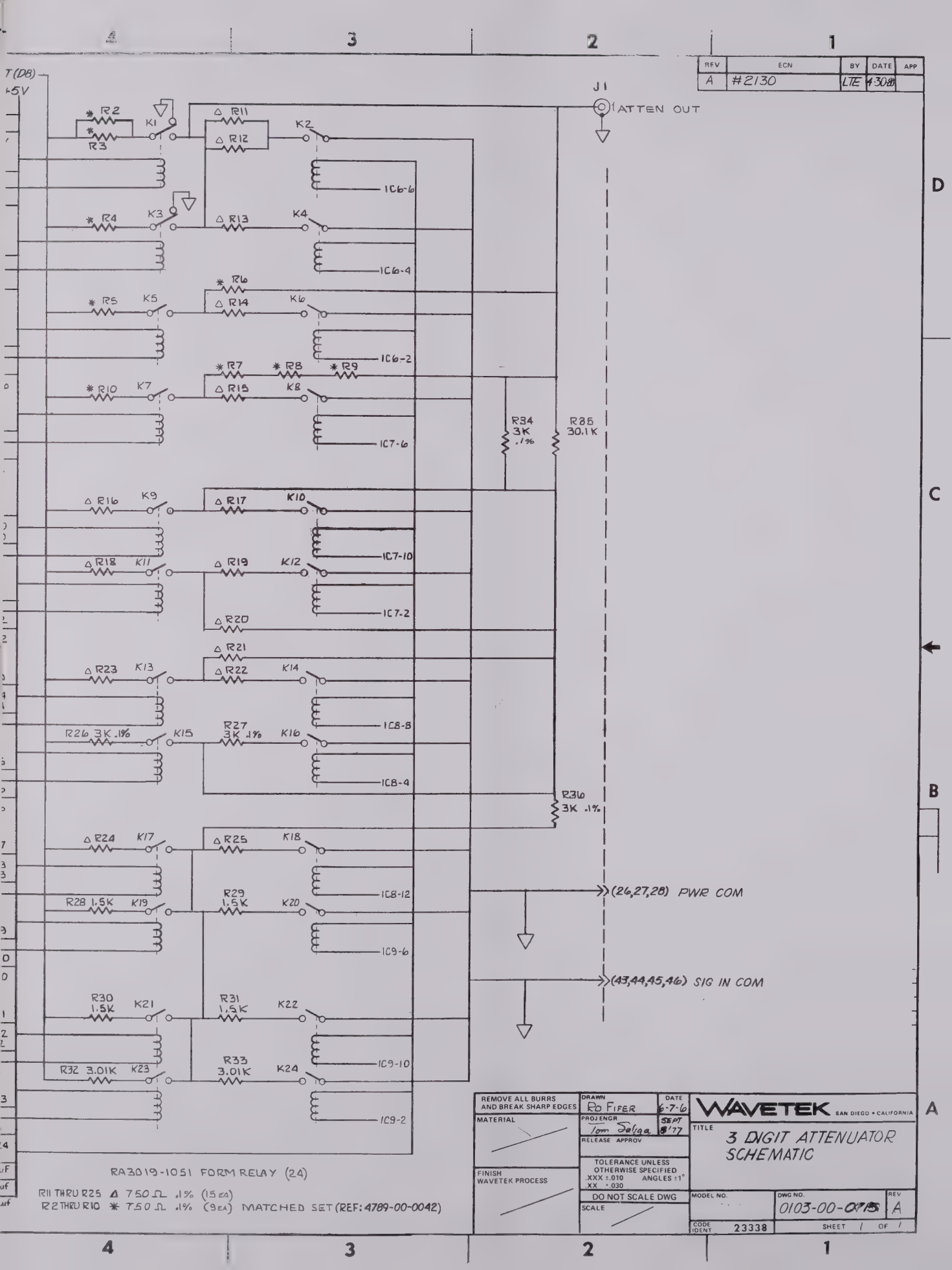
SUB ASSY #3	ASSEMBLY NO. 1208-00-0593 PAGE: 1	REV D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PWR AMPL SUB ASSY #3
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 172B	DWG NO 1208-00-0593 REV D
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A 3894

DEBCO BUSINESS FORMS PRINTING, INC. 2187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IC8-12
R28 1.5K
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R30
1.5K
K21
R31
1.5K
K22
IC9-10
R32 3.01K
K23
R33
3.01K
K24
IC9-2
(26,27,28) PWR COM
(43,44,45,46) SIG IN COM
RA3019-1051 FORM RELAY (24)
R11 THRU R25 Δ 750Ω .1% (15 EA)
R2 THRU R10 * 750Ω .1% (9 EA) MATCHED SET (REF: 4789-00-0042)
REV
ECN
BY
DATE
APP
A
#2130
LTE
4-30-81
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN
Ro Fifer
DATE
6-7-6
PROJ ENGR
Tom Saliga
SEPT 8'77
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
.XXX ±.010 ANGLES ±1°
.XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
3 DIGIT ATTENUATOR SCHEMATIC
MODEL NO.
DWG NO.
0103-00-0715
REV
A
CODE IDENT
23338
SHEET 1 OF 1

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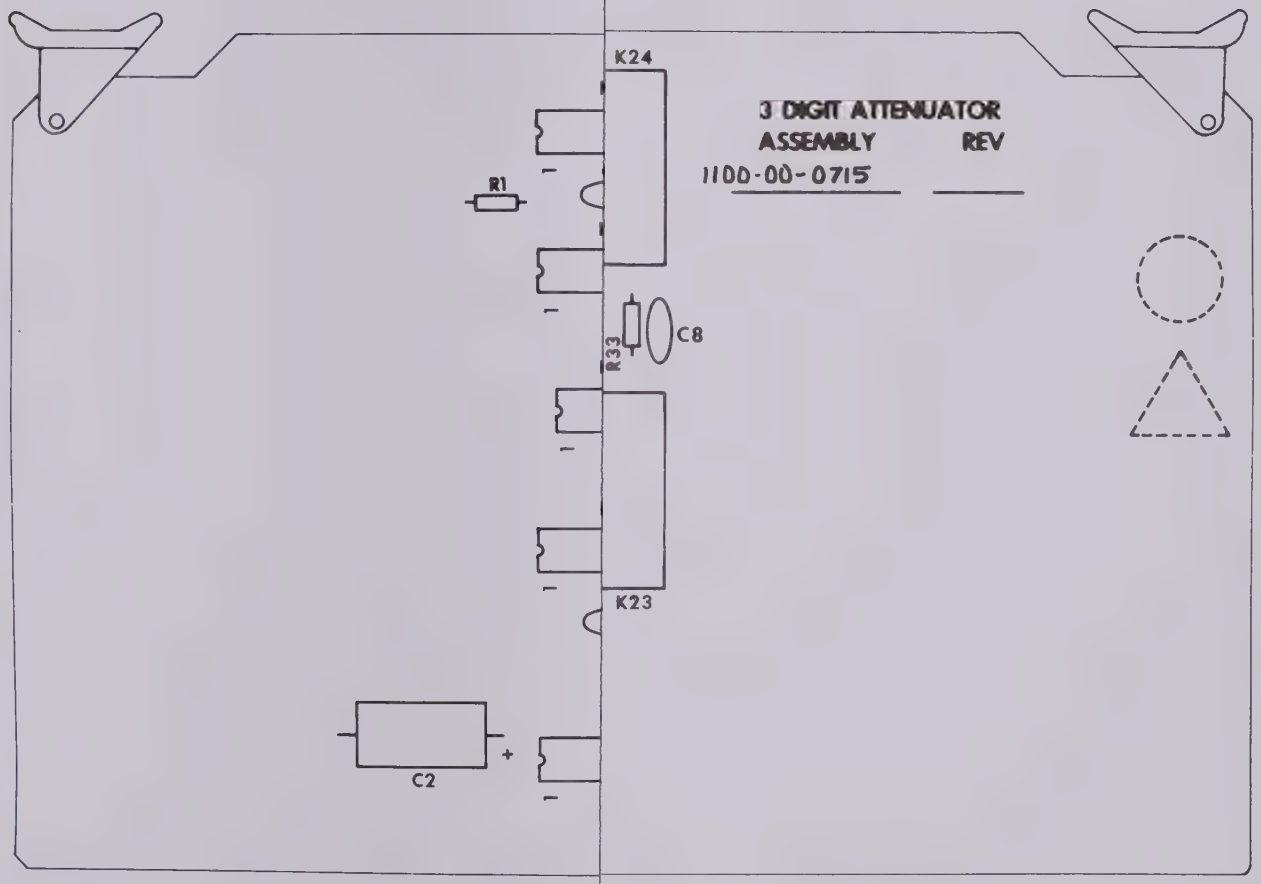


1100-00-0715

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: 3 DIGIT ATTENUATOR PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO: 172B; DWG NO: 0101-00-0715; REV:
	DO NOT SCALE DWG		CODE IDENT: 23338; SHEET 1 OF 1
	SCALE		

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, 3RD DIGIT	0101-00-0715	WVTK	0101-00-0715	1
NONE	SCHEMATIC, 3RD DIGIT	0103-00-0715	WVTK	0103-00-0715	1
C6 C7	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	2
C1 C3 C4 C5 C8	CAP, CER, MN, .01MF, 50V	CACD2Z5U103Z100A	CORNG	1500-01-0310	5
C2	CAP, ELECT, 100MF, 16V	500D1070016DC7	SPRAG	1500-31-0101	1
NONE	3RD DIGIT ATTEN BD	1700-00-0715	WVTK	1700-00-0715	1
J1	CONN	27-848	AMPH	2100-07-0011	1
NONE	PC BD EJECTOR	103 VIOLET	CALMK	2800-07-0015	2
NONE	TRANSIPAD	10123N	METRS	2800-11-0003	2
NONE	BALUN CORE	2873000902	FARIT	3100-00-0002	2
K10 K11 K12 K13 K14 K15 K16 K17 K18 K19 K2 K20 K21 K22 K23 K24 K4 K5 K6 K7 K8 K9	RELAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	22
K1 K3	RELAY, REED, FORM-C	RA3020-1051	ETROL	4500-00-0009	2
R26 R27 R34 R36	RES, MF, 1/8W, .1%, 3K	RN55E-3001B	MEPCO	4701-02-3001	4
R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25	RES, MF, 1/8W, .1%, 750	RN55E-7500B	MEPCO	4701-02-7500	15
R28 R29 R30 R31	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	4

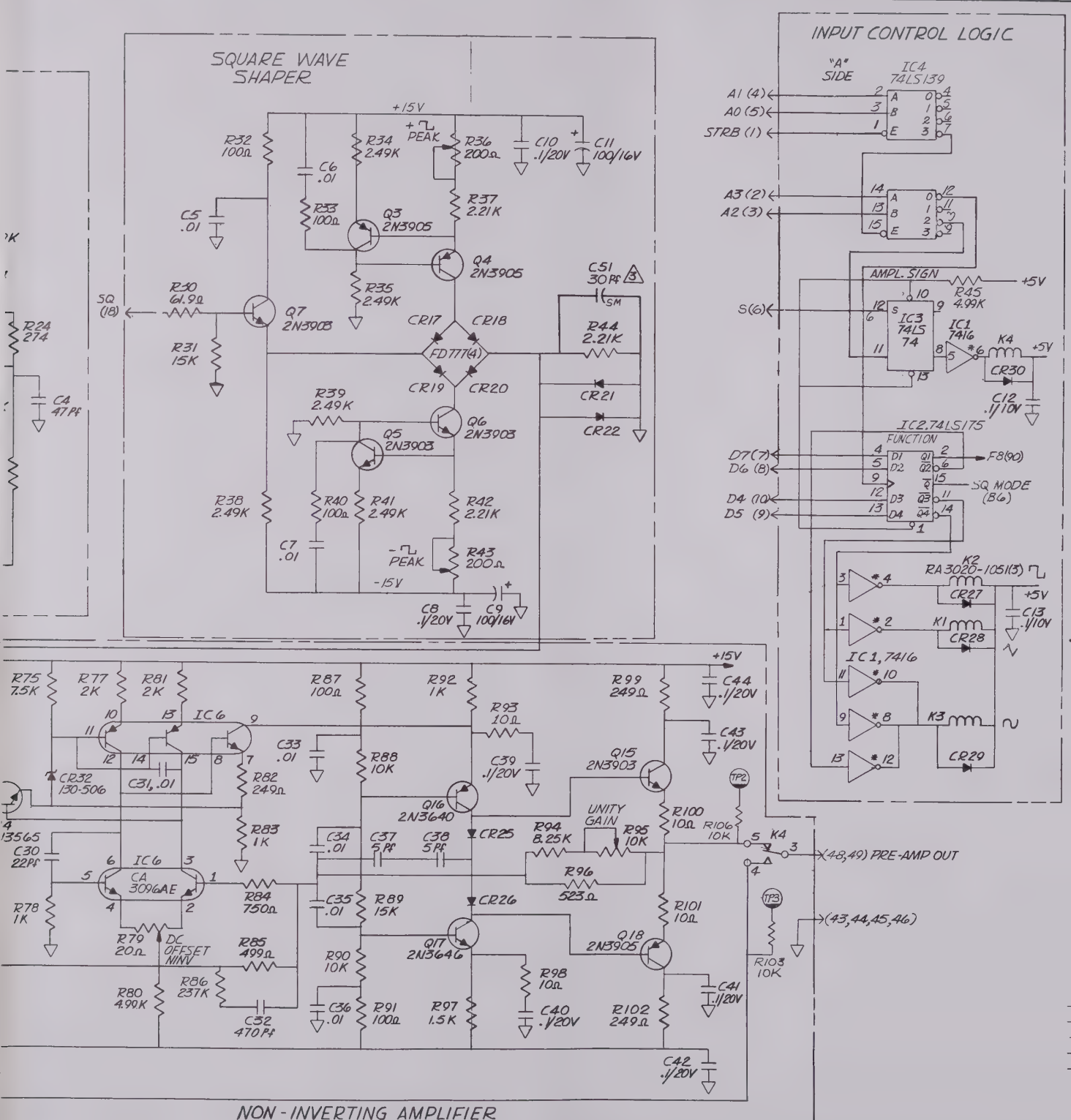
WAVETEK PARTS LIST | TITLE: PCA, 3 DIGIT ATTEN | ASSEMBLY NO. 1100-00-0715 | PAGE: 1 | REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R32 R33	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	2
R35	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
R1	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
R10 R2 R3 R4 R5 R6 R7 R8 R9	RES, SET, 9-750, 1/8W QTY: 9: 4701-02-7500	4789-00-0042	WVTK	4789-00-0042	1
CR5 CR1 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR21 CR22 CR23 CR24 CR3 CR4 CR6 CR7 CR8 CR9	DIODE	1N4148	FAIR	4807-02-6666	24
IC5	IC	74LS00	TI	8000-74-0010	1
IC6 IC7 IC8 IC9	IC	74LS05	TI	8000-74-0510	4
IC4	IC	74LS139	SIG	8007-41-3910	1
IC1 IC2 IC3	IC	74LS175	TI	8007-41-7510	3

WAVETEK PARTS LIST | TITLE: PCA, 3 DIGIT ATTEN | ASSEMBLY NO. 1100-00-0715 | PAGE: 2 | REV A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, 3 DIGIT ATTEN
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 172B / DWG NO 1100-00-0715 / REV A
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		

REV	ECN	BY	DATE	APP



△3 SQUARE WAVE ABERRATION TRIM CAP.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 6-28-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Selga	SEPT 7'77	TITLE SCHEMATIC FUNCTION/PRE-AMP.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO	DWG NO 0103-00-0707 REV F
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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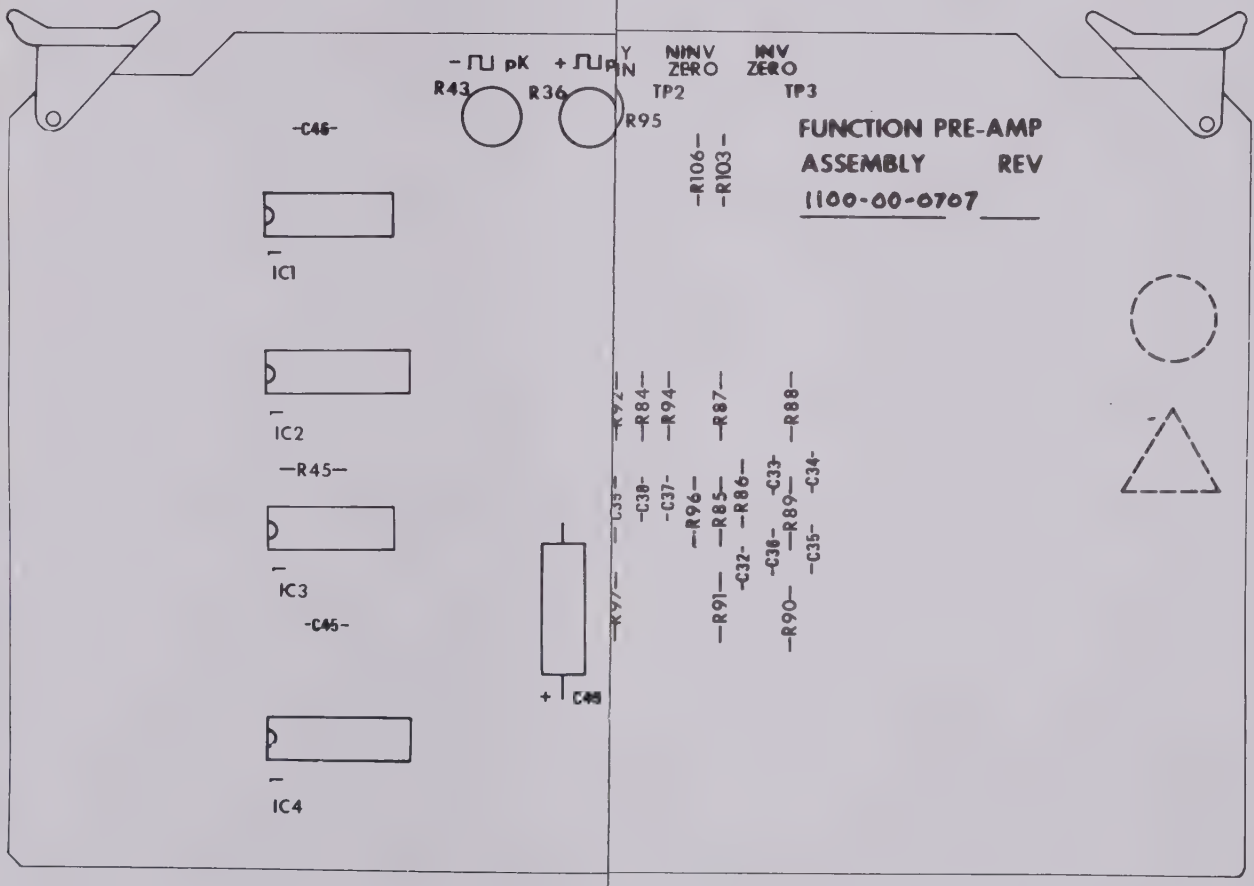

1100-00-0707

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: FUNCTION / PREAMP PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		MODEL NO 172B / DWG NO 0101-00-0707 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

REV	ECN	BY	DATE	APP

IQ-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
55D-1212F	TRW	4701-03-1212	4
55D-1302F	TRW	4701-03-1302	1
55D-1501F	TRW	4701-03-1501	2
55D-1502F	TRW	4701-03-1502	5
55D-1652F	TRW	4701-03-1652	3
55D-2001F	TRW	4701-03-2001	6
55D-21R5F	TRW	4701-03-2159	2
55D-2211F	TRW	4701-03-2211	3
55D-2373F	TRW	4701-03-2373	1
55D-2490F	TRW	4701-03-2490	7
55D-2491F	TRW	4701-03-2491	5
55D-2492F	TRW	4701-03-2492	2
55D-2740F	TRW	4701-03-2740	1
55D-3010F	TRW	4701-03-3010	2
55D-3160F	TRW	4701-03-3160	1
55D-33R2F	TRW	4701-03-3329	1

IQ-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
55D-3920F	TRW	4701-03-3920	2
55D-4990F	TRW	4701-03-4990	3
55D-4991F	TRW	4701-03-4991	3
55D-4992F	TRW	4701-03-4992	1
55D-5230F	TRW	4701-03-5230	1
55D-61R9F	TRW	4701-03-6199	1
55D-68R1F	TRW	4701-03-6819	1
55D-7500F	TRW	4701-03-7500	2
55D-7501F	TRW	4701-03-7501	2
55D-8251F	TRW	4701-03-8251	1
4581	MICRO	4801-01-4581	2
0777	FAIR	4807-02-0777	4
6148	FAIR	4807-02-6666	11
2-2811	HP	4809-02-2811	2
8-500-98	WVTK	4898-00-0010	2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR7 CR8 CR9					
Q13 Q14	TRANS	2N3565	FAIR	4901-03-5650	2
Q16 Q9	TRANS	2N3640	FAIR	4901-03-6400	2
Q11 Q17 Q8	TRANS	2N3646	NSC	4901-03-6460	3
Q10 Q15 Q2 Q5 Q6 Q7	TRANS	2N3903	NSC	4901-03-9030	6
Q1 Q12 Q18 Q3 Q4	TRANS	2N3905	ITT	4901-03-9050	5
RT1	THERMISTER	LB12J2	FNWL	5300-00-0002	1
IC5 IC6	IC	CA-3096AE	RCA	7000-30-9600	2
IC1	IC	7416	SIG	8000-74-1600	1
IC3	IC	74LS74	TI	8000-74-7410	1
IC4	IC	74LS139	SIG	8007-41-3910	1
IC2	IC	74LS175	TI	8007-41-7510	1

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, FUNCTION BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 172B / DWG NO 1100-00-0707 / REV F
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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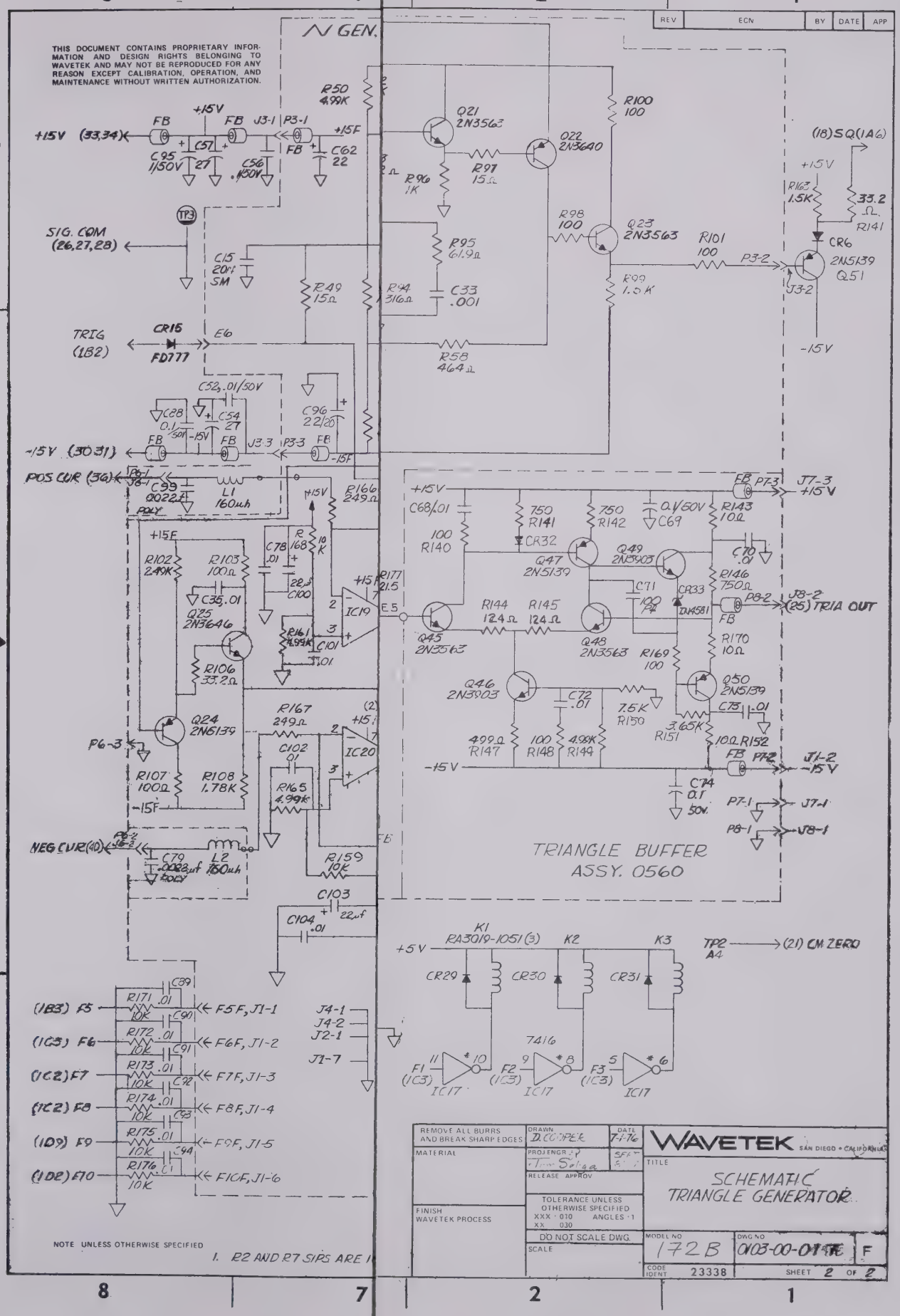
REV	ECN	BY	DATE	APP
A	ENG IMDR'L	RLF	8-22-77	
B	ECN 1657, 1701	RD	7-27-78	
	2921, 3552 (CL III)	DC	2-1-83	
C	3555	DC	2-3-83	
D	3937	SC	9-23-83	
E	4682	DAM	6-11-85	
F	6097	SC	12-2-85	

S (6A)
A3 (2A)
A2 (3A)
STRB (1A)
A3 A2 STRB
B7
F10 (2A8)
+15V
F9 (2A8)
+15V
A1 (4A)
A0 (5A)
A0 A1
B7
IC1
74LS139
F8 (2A8)
+15V
F7 (2A8)
+15V
+5V (19,20)
FB
C68 .1/10V
C1 27 35V
C2
C3 .01/50
C4 .01/50
C5 .01/50
C6 .01/50
-5V
COMMON (22,23,24)
Q1
2N2905A
D0 (14A)
D1 (13A)
D2 (12A)
CONTROL LOGIC
TRIGGER CIRCUIT
45
47
49
IC8
74LS139
A3 (D7)
A2 (D7)
STRB (D7)
A1 (C7)
A0 (C7)
R31 100Ω
C13 .01/50V
TRIG (2C7)
GEN OUT (B5)
(44) GEN OUT
SYNC OUT (B5)
(46) SYNC OUT
R116 30.1Ω
Q7 2N3646
C75 .01μF 50V
R153 4.99K
Q41 2N3565 (2)
Q52
R154 10K
R156 100Ω
CR14 FD777
+15V
P6-4
J6-4
C76 .01
P6-1
P6-3
R179 100Ω
(38) CI
GEN. TRI. GEN ASSY.-0559
+5V
MAN TRIG 48
R15 10K
R16 10K
TRIG IN 50
R17 499Ω
CR3
CR5
CR4 IN4732
MOTHER BOARD

NOTE. UNLESS OTHERWISE SPECIFIED
LAST REF. DESIGNATORS USED:
R181 · C105 · CR39 · IC20
L2 · K4 · Q53
2) ALL

BREAK SHARP EDGES	DRAWN D. COONEY	DATE 4-3-78	WAVETEK SAN DIEGO, CALIFORNIA
	PROJ. ENGR		TITLE: SCHEMATIC TRIANGLE GENERATOR
	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 172B
	DO NOT SCALE DWG		DWG NO 0103-00-0714 REV F
	SCALE		CODE IDENT. 23338 SHEET 1 OF 2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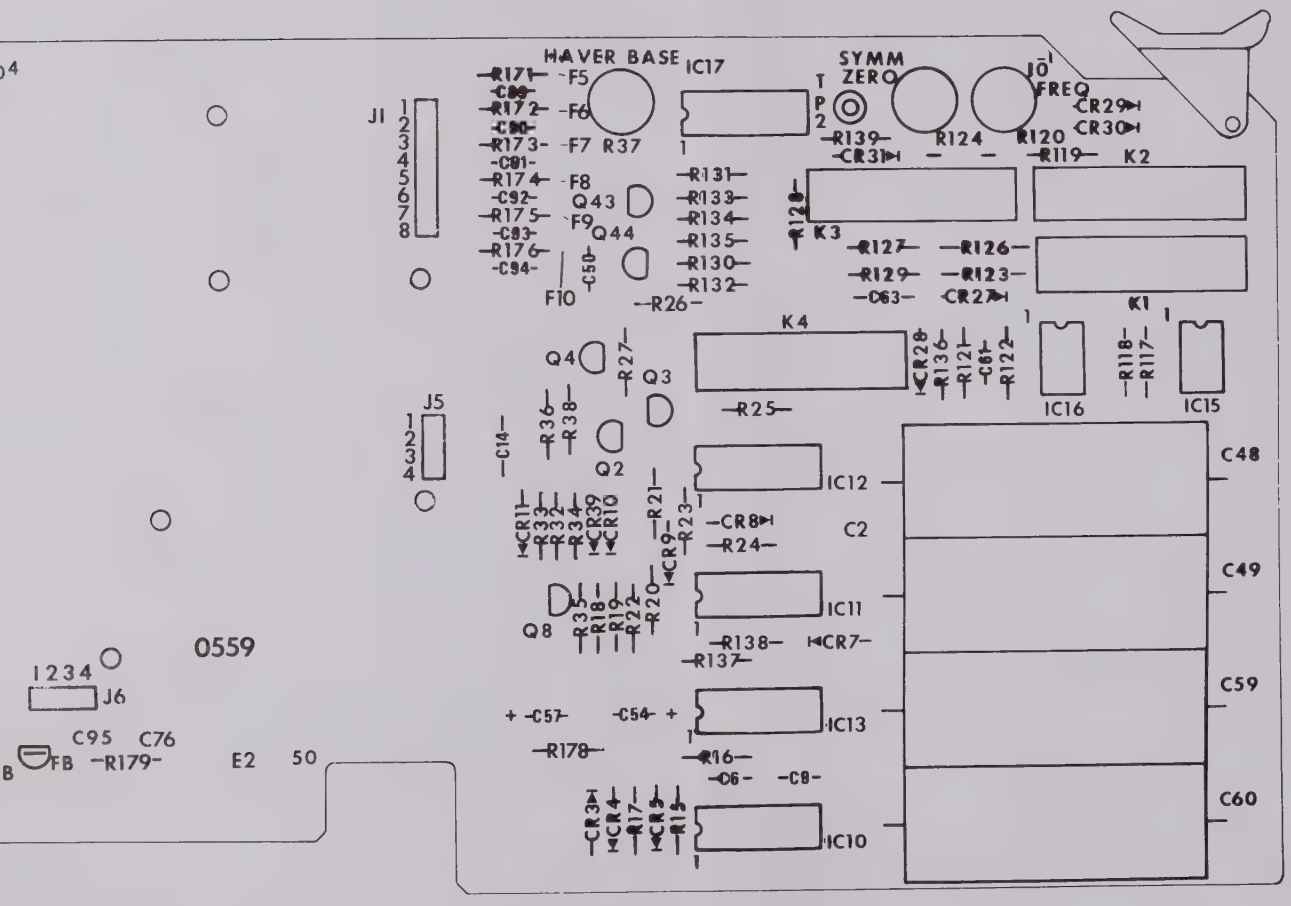
REV ECN BY DATE APP
N GEN.
+15V (33,34)
SIG. COM (26,27,28)
TRIG (1B2)
CR15 FD777
-15V (30,31)
POS CUR (36)
NEG CUR (40)
R50 4.99K
Q21 2N3563
Q22 2N3640
R100 100
R97 15Ω
R96 1K
R98 100
Q23 2N3563
R101 100
R95 61.9Ω
R99 1.0K
R49 15Ω
R54 316Ω
C33 .001
R58 464Ω
C15 20pf SM
(18) SQ (1A6)
R163 1.5K
33.2Ω R141
CR6
2N5139 Q51
P3-2
J3-2
C52 .01/50V
C96 22/20
C28 0.1/50V
C54 27
C62 22
C56 .1/50V
C57 27
C95 1/50V
L1 160μh
L2 150μh
C99 .0022
R166 249Ω
R168 10K
C78 .01
C100 22μf
R102 2.49K
R103 100Ω
C35 .01
Q25 2N3646
R106 33.2Ω
Q24 2N5139
R107 100Ω
R108 1.78K
R161 4.99K
C101 .01
IC19
R177 21.5
R167 249Ω
C102 .01
R165 4.99K
IC20
R159 10K
C103 22μf
C104 .01
P6-3
P6-2
TRIANGLE BUFFER ASSY. 0560
+15V C68 .01
100 R140
750 R141
750 R142
0.1/50V C69
R143 10Ω
CR32
Q47 2N5139
Q49 2N3903
C70 .01
C71 100pf
CR33 1N4581
R146 750Ω
P8-2
J8-2 (25) TRIA OUT
R144 124Ω
R145 124Ω
Q45 2N3563
Q48 2N3563
R169 100
R170 10Ω
Q46 2N3903
C72 .01
7.5K R150
Q50 2N5139
C75 .01
499Ω R147
100 R148
4.99K R149
3.65K R151
10Ω R152
C74 0.1 50V
P7-2
J1-2 -15V
P7-1
J7-1
P8-1
J8-1
P7-3
J7-3 +15V
K1 RA3019-1051 (3)
K2
K3
+5V
CR29
CR30
CR31
TP2 A4
(21) CM ZERO
7416
F1 (1C3) IC17
F2 (1C3) IC17
F3 (1C3) IC17
(1B3) F5
(1C3) F6
(1C2) F7
(1C2) F8
(1D3) F9
(1D2) F10
R171 10K
R172 10K
R173 10K
R174 10K
R175 10K
R176 10K
F5F, J1-1
F6F, J1-2
F7F, J1-3
F8F, J1-4
F9F, J1-5
F10F, J1-6
J4-1
J4-2
J2-1
J1-7
NOTE UNLESS OTHERWISE SPECIFIED
1. R2 AND R7 SIPS ARE
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER
DATE 7-7-76
PROJENGR Tom Salga
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG.
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC TRIANGLE GENERATOR
MODEL NO 172B
DWG NO 0103-00-01 REV F
CODE IDENT 23338
SHEET 2 OF 2



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: TRIANGLE GENERATOR PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± XX ± .030		MODEL NO: 172B
	DO NOT SCALE DWG		DWG NO: 0101-00-0714
	SCALE		REV
			CODE IDENT: 23338
			SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART
NONE	ASSY DRWG, TRI GEN	0101-00-0714
NONE	SCHEMATIC, TRI GEN	0103-00-0714
NONE	HYS. SWITCH TRI GEN	172-558
NONE	TRIGGER TRI GEN	172-559
NONE	BUFFER AMP TRI GEN	172-560
NONE	SHIELD	1400-00-6651
NONE	SHIELD	1400-00-6661
NONE	SHIELD	1400-00-6671
NONE	SHIELD	1400-00-6681
C61 C9	CAP, CER, 100PF, 1KV	DD-101
C2 C3 C4 C5 C50 C52 C6 C76 C80 C89 C90 C91 C92 C93 C94	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z1C
C14 C63 C68 C7 C8	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z05
C59 C60	CAP, POLYC, 5MF, 100V	C1A505F
C1 C54 C57	CAP, TANT, 27MF, 35V	196D276X0035TE
C56 C88 C95	CAP, CER, .1MF, 50V	D043BX104MP
NONE	SHIELD, COVER TRI. GEN	1700-00-0625
NONE	TRI GEN. CAP MULT BD	1700-00-0714

WAVETEK PARTS LIST	TITLE PCA, TRI GEN CAP MULT	ASS 110 PAG

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART
NONE	PIN, MALE	61182-2
NONE	CONN PIN, MALE (VOM-EA PIN)	CA-836SP-100-2
NONE	STANDOFF, SWAGE .750 H, .187 DIA 2-56, .062 MAT'L	SS168-1D-5A
NONE	PC BD EJECTOR	103 GREEN
NONE	TRANSIPAD	10123N
NONE	SCREW, 2-56X1/4 NYLON	2-56X1/4 NYLON
NONE	BALUN CORE	2873000902
K1 K2 K3	RELAY, REED, FORM-A	RA3019-1051
K4	RELAY, REED, FORM-C	RA3020-1051
R120 R37	POT, TRIM, 1K	91AR1K
R124	POT, TRIM, 20K	91AR20K
R128	RES, MF, 1/8W, .1%, 10K	RN55E-1002B
R127	RES, MF, 1/8W, .1%, 100K	RN55E-1003B
R179 R21	RES, MF, 1/8W, 1%, 100	RN55D-1000F
R118 R23 R32 R4	RES, MF, 1/8W, 1%, 1K	RN55D-1001F
R122 R139 R15 R16	RES, MF, 1/8W, 1%, 10K	RN55D-1002F

WAVETEK PARTS LIST	TITLE PCA, TRI GEN CAP MULT	ASS 110 PAG

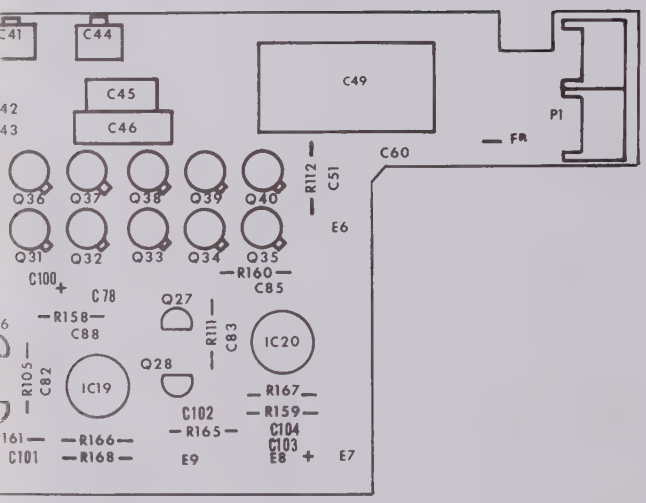
PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TRANS	2N3646	NSC	4901-03-6460	1
TRANS	2N3903	NSC	4901-03-9030	1
TRANS	2N5139	FAIR	4901-03-1390	5
IC	MLM339P	MOT	7000-03-3900	3
IC, OP-AMP	LF356N	NSC	7000-03-5600	2
IC	7416	SIG	8000-74-1600	3
IC	7474	TI	8000-74-7400	1
IC	74LS132	TI	8007-41-3210	1
IC	74LS139	SIG	8007-41-3910	2
IC	74LS145	SIG	8007-41-4510	2
IC	74LS175	TI	8007-41-7510	2

I GEN CAP MULT	ASSEMBLY NO. 1100-00-0714 PAGE: 5	REV C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
	RELEASE APPROV		PARTS LIST PCA, TRI GEN CAP MULT
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 172B / DWG NO 1100-00-0714 / REV C
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

B:SHOP.GRAPH.CS/ACCUPRESS
REORDER NO. A-3894



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: HYSTERESIS SW ASSY, TRI GEN
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO
	SCALE		DWG NO 0101-00-0558 REV
			CODE IDENT 23338 SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO
NONE	ASSY DRWG, HYS SWITCH	0101-00-0558
NONE	SCHEMATIC, TRI GEN	0103-00-0714
C22T C23 C28 C29T C64 C97 C98	CAP, CER, 5PF, 1KV	DD-050 LONG LEAD
C30 C31	CAP, CER, 100PF, 1KV	DD-101 LONG LEAD
C33 C60 C85 C88	CAP, CER, .001MF, 1KV	DD-102 LONG LEAD
C101 C102 C104 C16 C17 C18 C19 C32 C35 C51 C78	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A
C25 C26	CAP, CER, 22PF, 1KV	DD-220 LONG LEAD
C81	CAP, MICA, 150PF, 500V	DM15-151J
C15 C40	CAP, MICA, 20PF, 500V	DM15-200J
C24 C27	CAP, MICA, 30PF, 500V	DM15-300J
C43T	CAP, MICA, 39PF, 500V	DM15-390J
C84	CAP, MICA, 68PF, 500V	DM15-680J
C42	CAP, MICA, 820PF, 300V	DM15-821F
C41 C44	CAP, VARI, 7-35PF, 250V	7S TRIKO-22, 7/3
C100 C103 C62 C96	CAP, TANT, 22MF, 15V	196D226X9015KA1

WAVETEK PARTS LIST

TITLE
HYS. SWITCH TRI GEN

ASSEMB
1208-

PAGE

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	1
RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	5
RES, MF, 1/8W, 1%, 3.65K	RN55D-3651F	TRW	4701-03-3651	1
RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
RES, MF, 1/8W, 1%, 4.32K	RN55D-4321F	TRW	4701-03-4321	2
RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	2
RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	3
RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	6
RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	3
RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	3
RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	1
DIODE	1N751A	FAIR	4801-01-0751	1
DIODE	1N4581	MICRO	4801-01-4581	1
DIODE	FD777	FAIR	4807-02-0777	11
DIODE	1N4148	FAIR	4807-02-6666	1

TCH TRI GEN | ASSEMBLY NO. 1208-00-0558 | REV G

PAGE: 4

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TRANS	2N3563	FAIR	4901-03-5630	5
TRANS	2N3640	FAIR	4901-03-6400	7
TRANS	2N3646	NSC	4901-03-6460	2
TRANS	2N5139	FAIR	4901-05-1390	1
TRANS	2N5460	MOT	4901-05-4600	1
TRANS	2N5485	MOT	4901-05-4850	1
TRANS	SD215DE	SIG	4902-00-2140	11
TRANS, M/PR, 2N5485 QTY: 2: 4901-05-4850	142-501-53	WVTK	4998-00-0009	1
IC, OP-AMP	LF356N	NSC	7000-03-3600	2
IC	CA3049T	RCA	7000-30-4900	1

TCH TRI GEN | ASSEMBLY NO. 1208-00-0558 | REV G

PAGE: 5

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS

NOTE UNLESS OTHERWISE SPECIFIED

DRAWN	DATE
PROJ ENGR	
RELEASE APPROV	

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
.XX ± .030

DO NOT SCALE DWG
SCALE

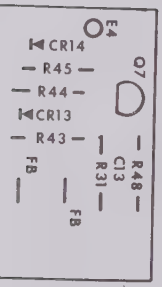
WAVETEK SAN DIEGO • CALIFORNIA

TITLE
PARTS LIST
HYS. SWITCH TRI GEN

MODEL NO	DWG NO	REV
172B	1208-00-0558	G

CODE IDENT 23338 | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3894



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY TRIGGER, TRIANGLE GEN. ASSY.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG		MODEL NO 172 / DWG NO 0101-00-0559 / REV
	SCALE		CODE IDENT 23338 / SHEET OF

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
ASSY DRWG, TRIGGER	0101-00-0559	WVTK	0101-00-0559	1
SCHEMATIC, TRI GEN	0103-00-0714	WVTK	0103-00-0714	1
CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	2
CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	1
CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	1
POLYC, .0022MF, 200V	192P22292	SPRAG	1500-42-2204	2
CAP, CER, .1MF, 50V	D045BX104MP	WSTCP	1509-90-0011	2
TRIGGER	1700-00-0559	WVTK	1700-00-0559	1
CHOKE, 160MH	1537-86	DLVAN	1800-00-0016	2
CONN	22-17-2042	MOLEX	2100-02-0065	2
SOCKET	5-330808-0	AMP	2100-03-0044	3
TRANSIPAD	10123N	METRS	2800-11-0003	2
BALUN CORE	2873000902	FARIT	3100-00-0002	2
RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	4
RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	1
RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	1
RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	1

R TRI GEN	ASSEMBLY NO. 1208-00-0559 PAGE: 1	REV C

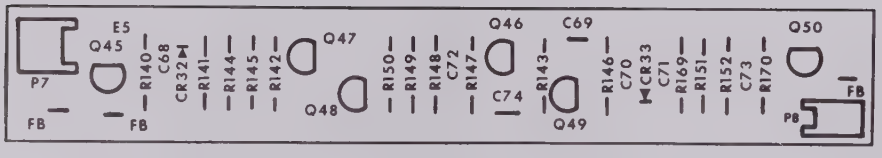
PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
RES, MF, 1/8W, 1%, 61.9	RN55D-61R9F	TRW	4701-03-6199	2
RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	2
DIODE	1N751A	FAIR	4801-01-0751	1
DIODE	FD777	FAIR	4807-02-0777	1
DIODE	1N4148	FAIR	4807-02-6666	1
TRANS	2N3565	FAIR	4901-03-3650	2
TRANS	2N3640	FAIR	4901-03-6400	1
TRANS	2N3646	NSC	4901-03-6460	2
TRANS, M/PR, 2N5485 QTY: 2: 4901-05-4850	142-501-53	WVTK	4998-00-0009	1

ER TRI GEN	ASSEMBLY NO. 1208-00-0559 PAGE: 2	REV C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE
	RELEASE APPROV		PARTS LIST TRIGGER TRI GEN
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ·010 ANGLES ·1 XX .030		
	DO NOT SCALE DWG	MODEL NO 172B	DWG NO 1208-00-0559 REV C
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894



1208-00-0560

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR		TITLE ASSEMBLY BUFFER AMPLIFIER TRIANGLE GENERATOR ASSY.	
	RELEASE APPROV			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030			
	DO NOT SCALE DWG		MODEL NO 172	DWG NO 0101-00-0560 REV
	SCALE		CODE IDENT 23338	SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
ASSY DRWG, BUFFER AMP	0101-00-0560	WVTK	0101-00-0560	1
SCHEMATIC, TRI GEN	0103-00-0714	WVTK	0103-00-0714	1
CAP, CER, 100PF, 1KV	DD-101 LONG LEAD	CRL	1500-01-0101	1
CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	4
CAP, CER, .1MF, 50V	DG45BX104MP	WSTCP	1509-90-0011	2
BUFFER AMP	1700-00-0560	WVTK	1700-00-0560	1
CONN	22-17-2022	MOLEX	2100-02-0061	1
CONN	22-17-2032	MOLEX	2100-02-0066	1
SOCKET	5-330808-0	AMP	2100-03-0044	1
TRANSIPAD	10123N	METRS	2800-11-0003	3
BALUN CORE	2873000902	FARIT	3100-00-0002	3
RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	3
RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	3
RES, MF, 1/8W, 1%, 124	RN55D-1240F	TRW	4701-03-1240	2
RES, MF, 1/8W, 1%, 3.65K	RN55D-3651F	TRW	4701-03-3651	1
RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	3

? AMP TRI GEN | ASSEMBLY NO. 1208-00-0560 | PAGE: 1 | REV A

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	1
DIODE	1N4381	MICRO	4801-01-4381	1
DIODE	1N4148	FAIR	4807-02-6666	1
TRANS	2N3563	FAIR	4901-03-5630	2
TRANS	2N3903	NSC	4901-03-9030	2
TRANS	2N5139	FAIR	4901-05-1390	2

R AMP TRI GEN | ASSEMBLY NO. 1208-00-0560 | PAGE: 2 | REV A

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN | DATE

PROJ ENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

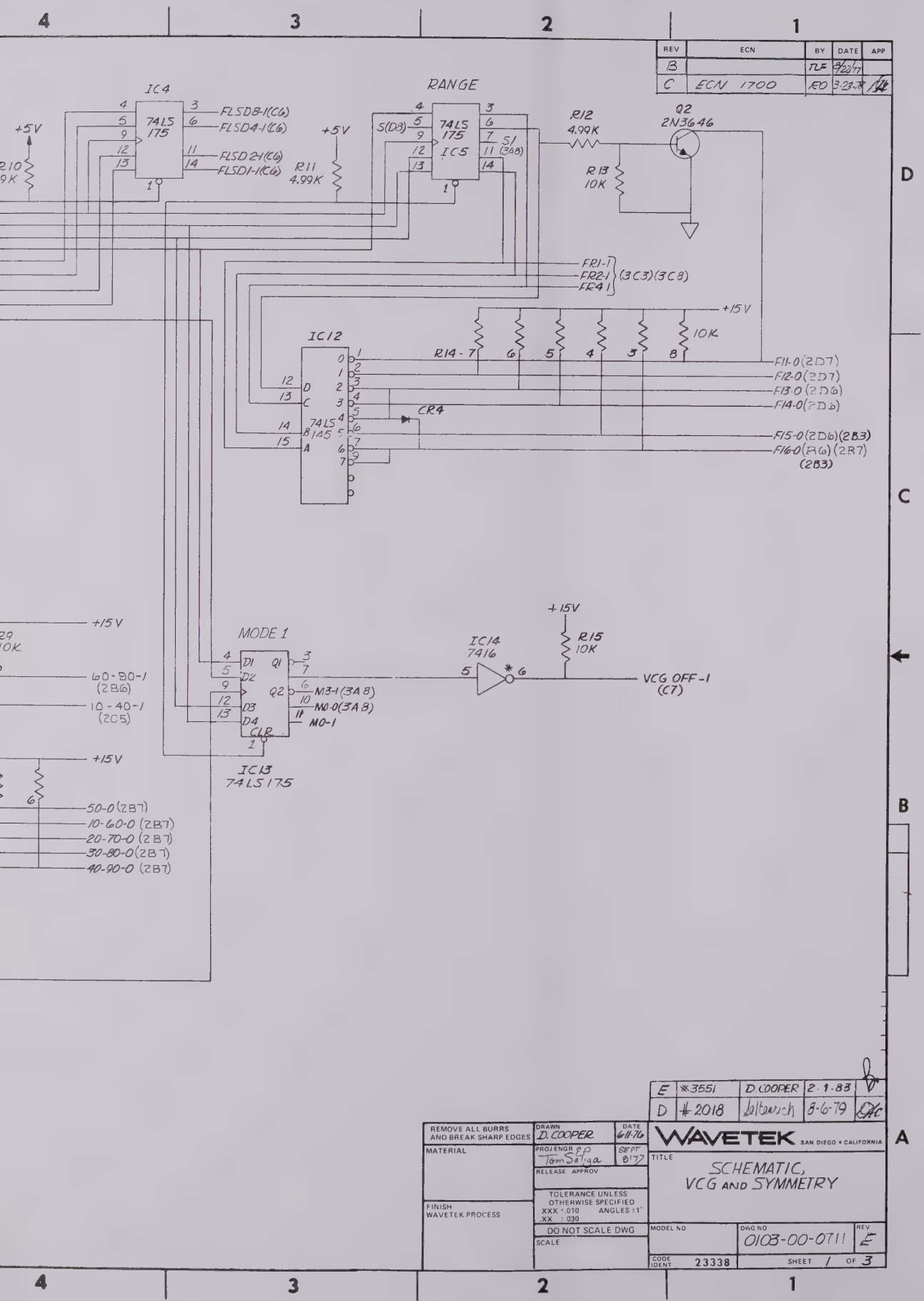
PARTS LIST
BUFFER AMP TRI GEN

MODEL NO 172B | DWG NO 1208-00-0560 | REV A

CODE IDENT 23338 | SHEET 1 OF

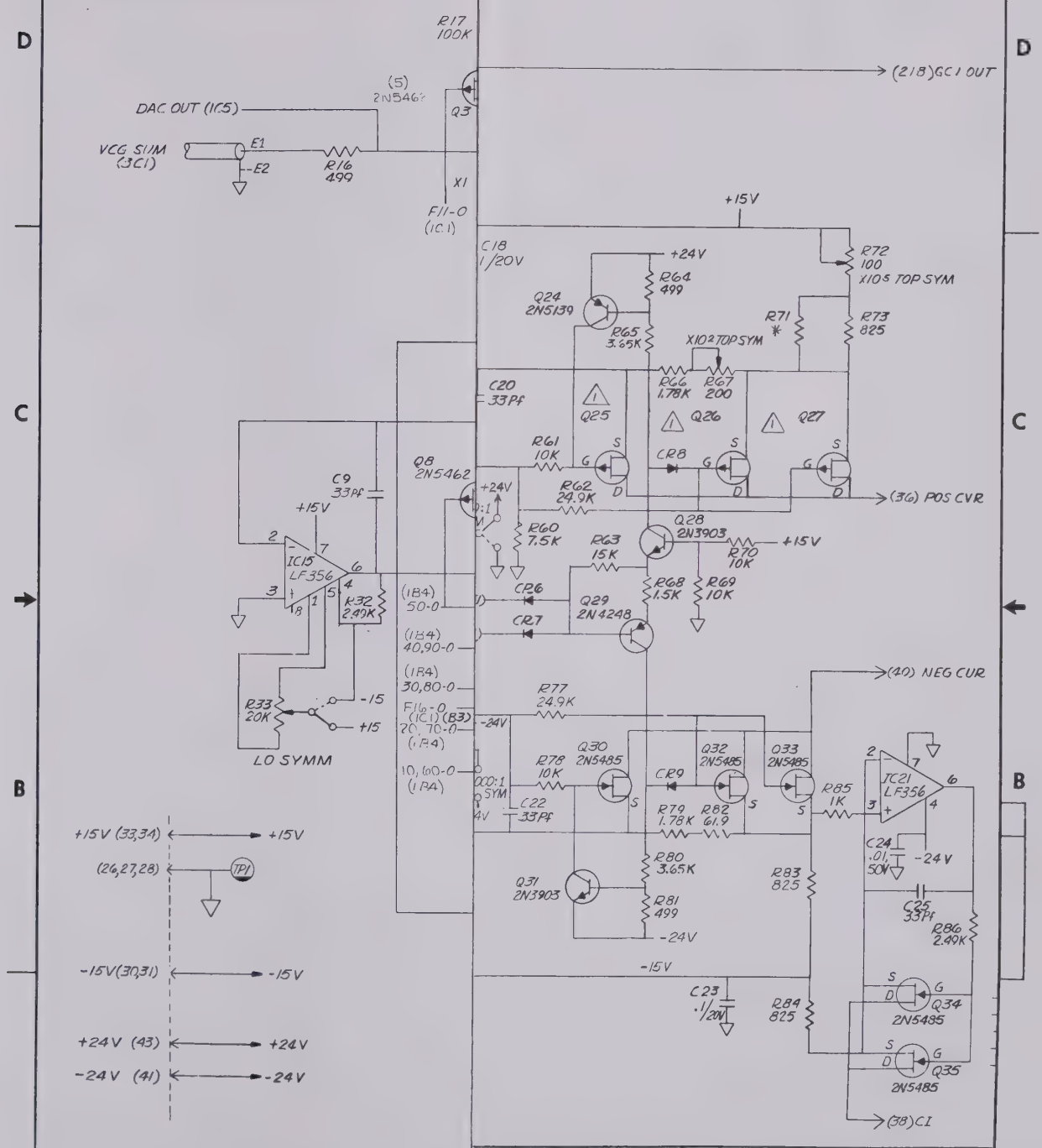
NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3894


4
3
2
1
REV | ECN | BY | DATE | APP
B | | TLF | 8/23/77 |
C | ECN 1700 | EO | 3.23.78 |
IC4
74LS 175
+5V
FLSD8-1(C6)
FLSD4-1(C6)
FLSD2-1(C6)
FLSD1-1(C6)
R11 4.99K
RANGE
S(D3)
IC5
R12 4.99K
Q2 2N3646
R13 10K
FR1-1
FR2-1
FR4-1
(3C3)(3C8)
+15V
IC12
74LS 8145
R14-7 6 5 4 3 8
10K
F11-0(2D7)
F12-0(2D7)
F13-0(2D6)
F14-0(2D6)
CR4
F15-0(2D6)(2B3)
F16-0(B6)(2B7)
(2B3)
MODE 1
IC13
74LS175
M3-1(3A8)
M0-0(3A8)
M0-1
IC14
7416
R15 10K
VCG OFF-1
(C7)
60-90-1
(2B6)
10-40-1
(2C5)
50-0(2B7)
10-60-0 (2B7)
20-70-0 (2B7)
30-80-0(2B7)
40-90-0 (2B7)
D
C
B
A
E | #3551 | D. COOPER | 2.1.83
D | #2018 | Baltzersen | 8-6-79
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER DATE 6-11-76
PROJ ENGR Tom Salga DEPT 817
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC, VCG AND SYMMETRY
MODEL NO
DWG NO 0103-00-0711
REV E
CODE IDENT 23338
SHEET 1 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

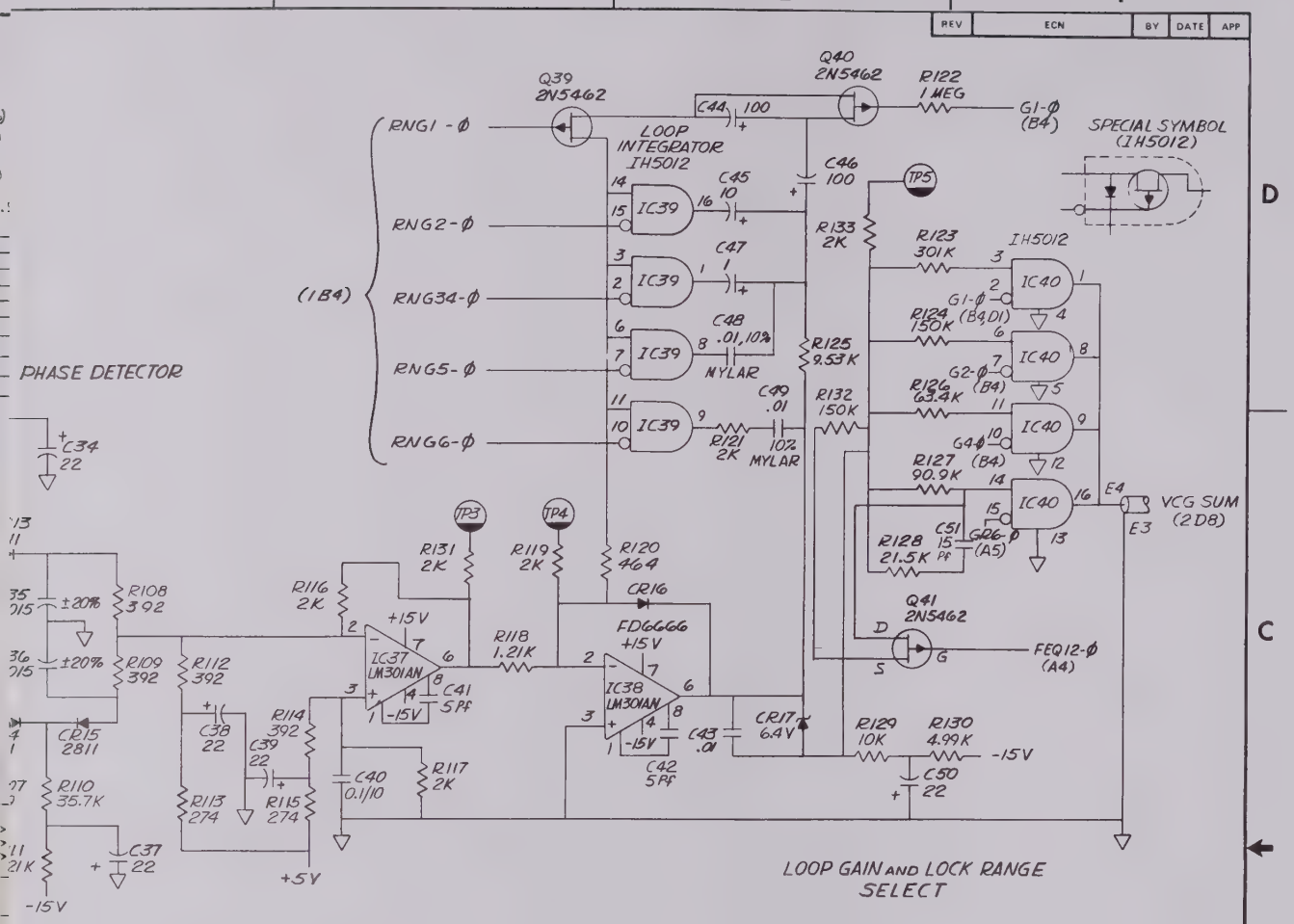
REV	ECN	BY	DATE	APP



LAST REF. DES. USED: T1, R133,

NOTE UNLESS OTHERWISE SPECIFIED △ 4998 00-0010

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 6-14-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Salga	SEPT 8'77	TITLE: SCHEMATIC - VCG & SYMMETRY
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX .030 ANGLES ±1	
	DO NOT SCALE DWG	MODEL NO	DWG NO 0103-00-0711 REV E
	SCALE	CODE IDENT 23338	SHEET 2 OF 3



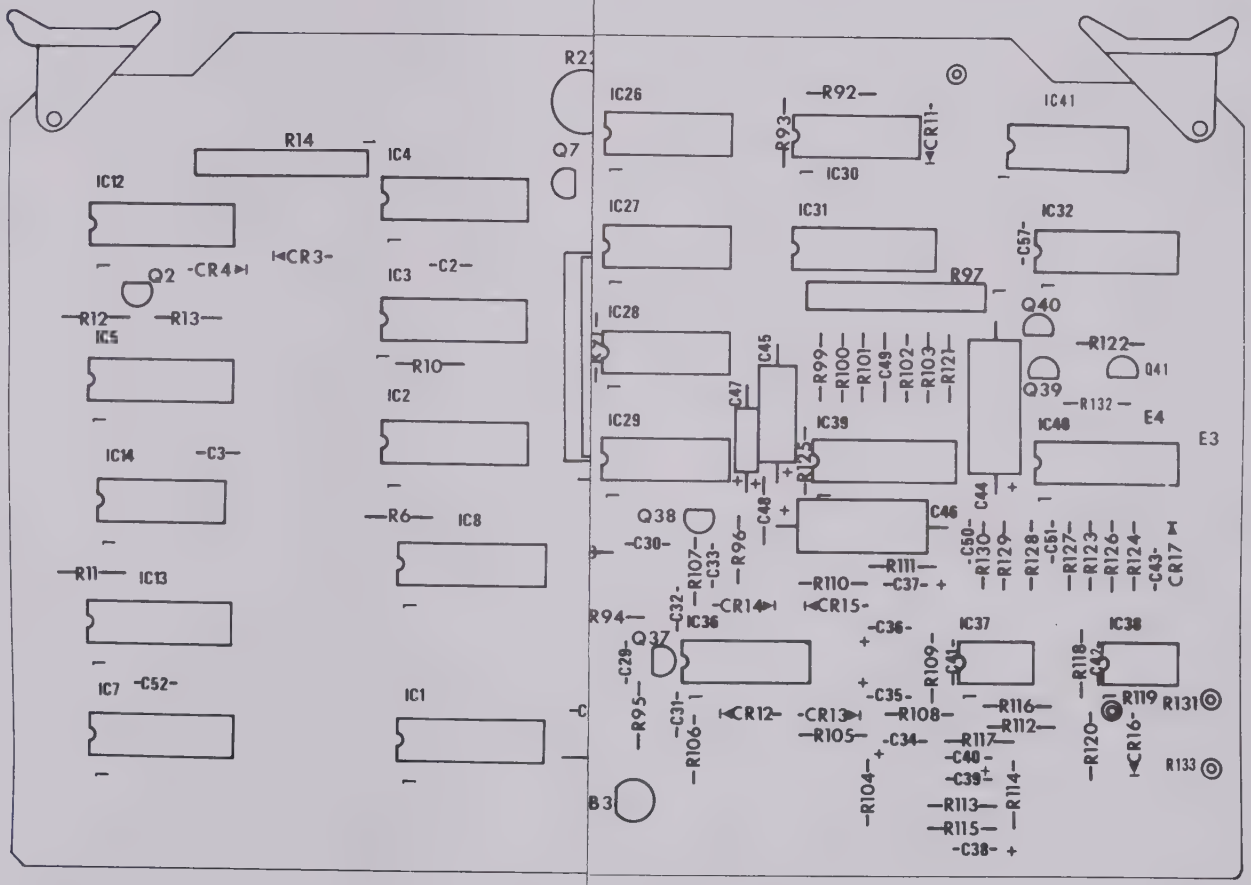
NOTES: TP3, TP4 MAY BE USED TO MEASURE PLL BANDWIDTH

TP5: AS PLL VARIES OVER LOCK RANGE; TP5 VARIES OVER ± 7 VDC

LAST REF. DES. USED:
T1, R133, C60, Q41, CR17, IC41, TP5, FB3

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D COOPER	DATE 5-5-77	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR Tom Saliga	SEPT 8/77	TITLE SCHEMATIC VCG AND SYMMETRY	
	RELEASE APPROV			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030			
	DO NOT SCALE DWG		MODEL NO.	DWG NO. 0103-00-0711 REV E
	SCALE		CODE IDENT 23338	SHEET 3 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



1100-00-0711

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: VCG & SYMMETRY PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 172B / DWG NO 0101-00-0711 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

REV	ECN	BY	DATE	APP

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT	REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
N55D-1002F	TRW	4701-03-1002	12	R100 R101 R102 R103 R122 R99	RES, MF, 1/4W, 1%, 1M	RN60D-1004F	TRW	4701-13-1004	6
N55D-10R0F	TRW	4701-03-1009	1	R14 R9 R97	RES MODULE	4310R-101-103	BOURN	4770-00-0008	3
N55D-1211F	TRW	4701-03-1211	3	CR17	DIODE	1N4581	MICRO	4801-01-4581	1
N55D-1501F	TRW	4701-03-1501	1	CR1 CR10 CR16 CR2 CR4 CR5 CR6 CR7 CR8 CR9	DIODE	1N4148	FAIR	4807-02-6666	10
N55D-1502F	TRW	4701-03-1502	7	CR11 CR12 CR13 CR14 CR15 CR3	DIODE	5082-2811	HP	4809-02-2811	6
N55D-1503F	TRW	4701-03-1503	2	Q2	TRANS	2N3646	NSC	4901-03-6460	1
N55D-1781F	TRW	4701-03-1781	2	Q28 Q31 Q36	TRANS	2N3903	NSC	4901-03-9030	3
N55D-2000F	TRW	4701-03-2000	1	Q37 Q38	TRANS	2N3905	ITT	4901-03-9050	2
N55D-2001F	TRW	4701-03-2001	8	Q29	TRANS	2N4248	FAIR	4901-04-2480	1
N55D-2052F	TRW	4701-03-2052	1	Q24	TRANS	2N5139	FAIR	4901-05-1390	1
N55D-2152F	TRW	4701-03-2152	1	Q1 Q10 Q11 Q12 Q14 Q15 Q17 Q18 Q19 Q20 Q21 Q23 Q3 Q39 Q4 Q40 Q41 Q5 Q6 Q7 Q8 Q9	TRANS	2N5462	MOT	4901-05-4620	22
N55D-2211F	TRW	4701-03-2211	5						
N55D-2490F	TRW	4701-03-2490	1	Q22 Q30 Q32 Q33 Q34 Q35	TRANS	2N5485	MOT	4901-05-4850	6
N55D-2491F	TRW	4701-03-2491	8	Q13 Q16	TRANS	SD215DE	SIG	4902-00-2140	2
N55D-2492F	TRW	4701-03-2492	2	Q25 Q26 Q27	TRANS, SEL, 2N5461	4998-00-0040	WVTK	4998-00-0040	3

ASSEMBLY NO. 1100-00-0711 REV F

PAGE: 3

WAVETEK PARTS LIST

TITLE PCA, VCG BD

ASSEMBLY NO. 1100-00-0711 REV F

PAGE: 5

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT	REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
					QTY: 1: 4901-05-4610				
N55D-2740F	TRW	4701-03-2740	2	IC37 IC38 IC6	IC	LM 301AN	NSC	7000-03-0100	3
N55D-3013F	TRW	4701-03-3013	2	IC15 IC16 IC17 IC18 IC19 IC20 IC21	IC, OP-AMP	LF356N	NSC	7000-03-5600	7
N55D-3572F	TRW	4701-03-3572	1	IC9	IC	AD563J	ANDEV	7000-05-6300	1
N55D-3651F	TRW	4701-03-3651	2	IC39 IC40	IC	IH5012	INTSL	8000-50-1200	2
N55D-3920F	TRW	4701-03-3920	4	IC29 IC30	IC	74LS00	TI	8000-74-0010	2
N55D-4640F	TRW	4701-03-4640	1	IC33	IC	7404	TI	8000-74-0400	1
N55D-4990F	TRW	4701-03-4990	5	IC14	IC	7416	SIG	8000-74-1600	1
N55D-4991F	TRW	4701-03-4991	6	IC41	IC	7426	TI	8000-74-2600	1
N55D-4992F	TRW	4701-03-4992	3	IC23	IC	74LS42B	SIG	8000-74-4210	1
N55D-61R9F	TRW	4701-03-6199	1	IC36	IC	MC12040	MOT	8001-20-4000	1
N55D-6342F	TRW	4701-03-6342	1	IC22	IC	74LS132	TI	8007-41-3210	1
N55D-6982F	TRW	4701-03-6982	2	IC1 IC7	IC	74LS139	SIG	8007-41-3910	2
N55D-7501F	TRW	4701-03-7501	2	IC10 IC11 IC12 IC31 IC32	IC	74LS145	SIG	8007-41-4510	5
N55D-8250F	TRW	4701-03-8250	3	IC34	IC	74LS151	TI	8007-41-5110	1
N55D-8251F	TRW	4701-03-8251	1	IC13 IC2 IC3 IC4 IC5 IC8	IC	74LS175	TI	8007-41-7510	6
N55D-9092F	TRW	4701-03-9092	1						
N55D-9531F	TRW	4701-03-9531	1						

ASSEMBLY NO. 1100-00-0711 REV F

PAGE: 4

WAVETEK PARTS LIST

TITLE PCA, VCG BD

ASSEMBLY NO. 1100-00-0711 REV F

PAGE: 6

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1 XX ± 030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

PARTS LIST
PCA, VCG BD

MODEL NO	DWG NO	REV
172B	1100-00-0711	F
CODE IDENT 23338	SHEET 1 OF 2	

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC	74LS196	SIG	8007-41-9610	5

CG BD

ASSEMBLY NO.
1100-00-0711

PAGE 7

REV F

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

NOTE UNLESS OTHERWISE SPECIFIED

DRAWN | DATE

PROJENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

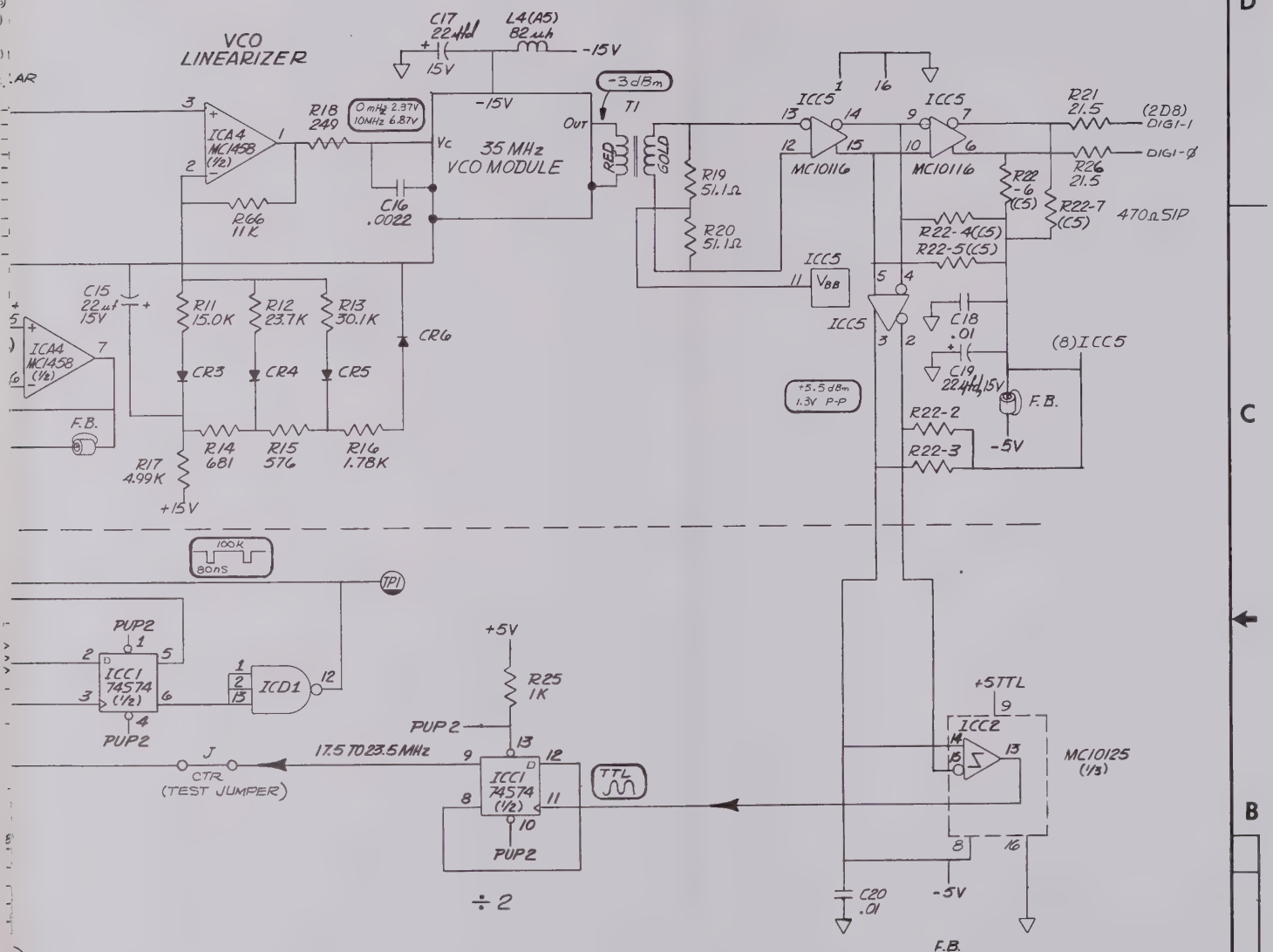
PARTS LIST
PCA, VCG BD

MODEL NO.	DWG NO.	REV
172B	1100-00-0711	F

CODE IDENT 23338 | SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A 3894

REV	ECN	BY	DATE	APP
D	R3 WAS 2K, ICC2-8&15 WERE COMMON, "SBL-1" WAS "MD108"	TLF	6/30/77	



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 7-6-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Salga	SEPT 7'77	TITLE SCHEMATIC DIG 1/MIXER PCB.
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG	MODEL NO.	DWG NO. 0103-00-0706 REV D
	SCALE	CODE IDENT 23338	SHEET 1 OF 2

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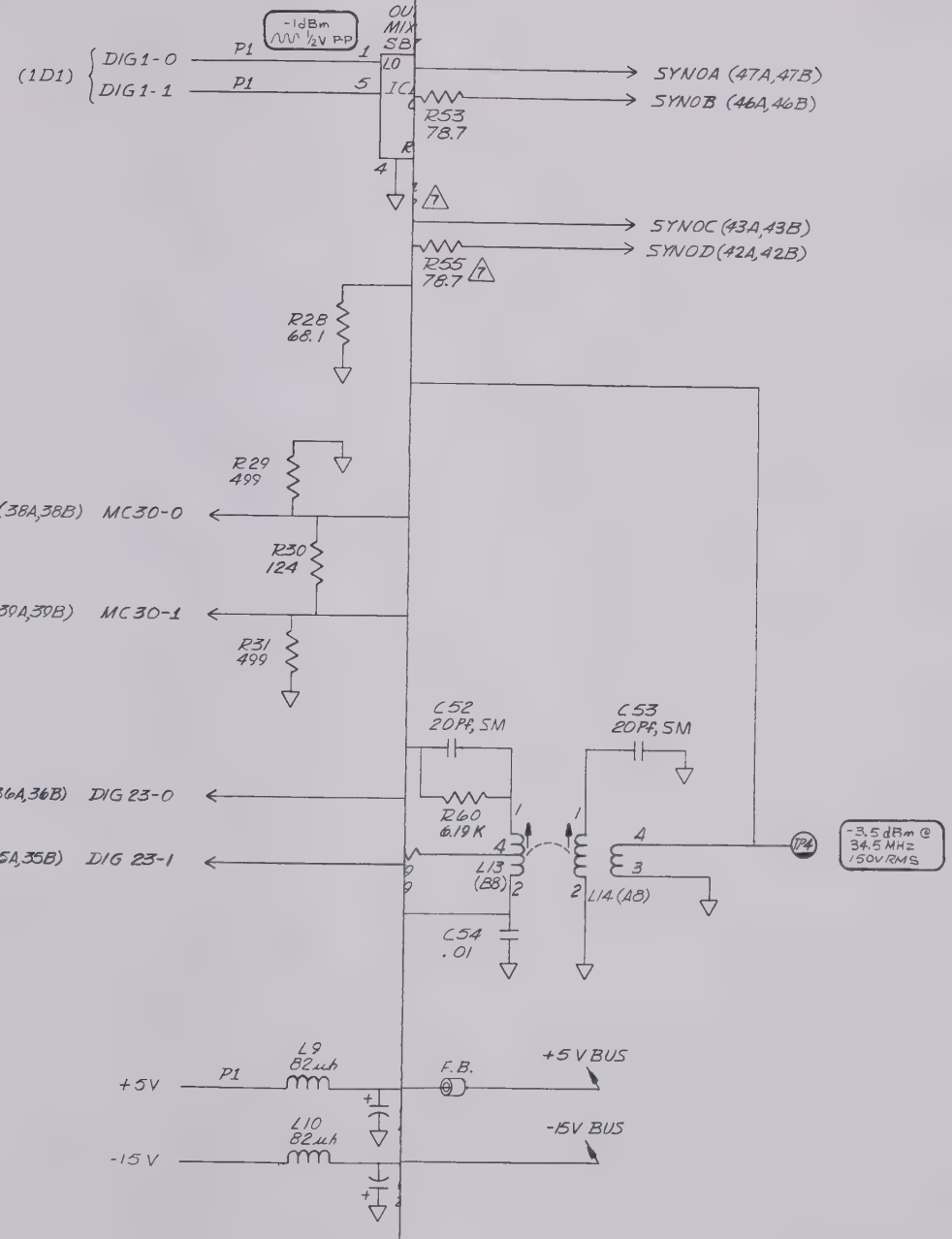
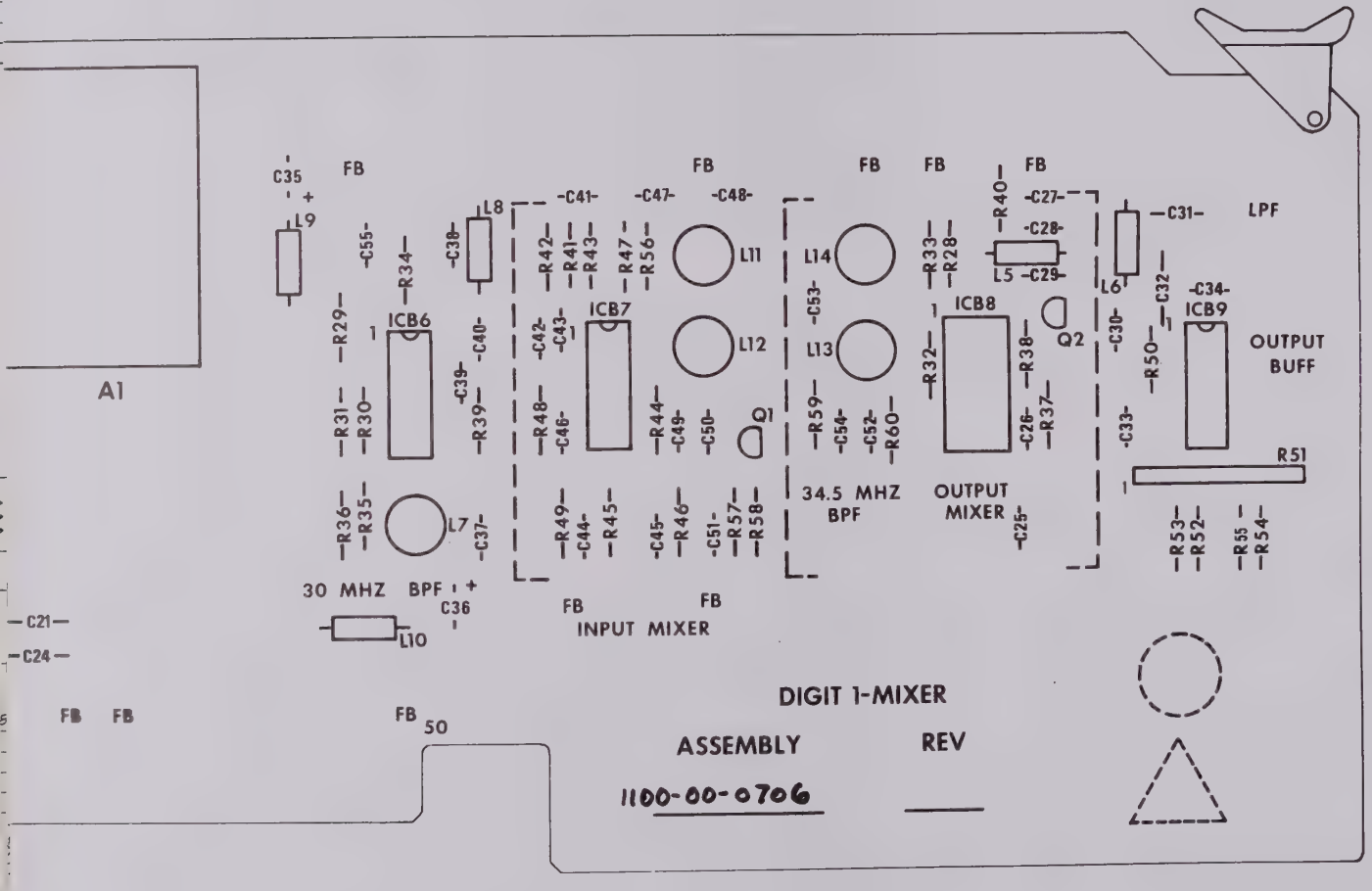
REV	ECN	BY	DATE	APP



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 76-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Seliga	SEPT 7'77	TITLE SCHEMATIC DIG 1/MIXER PC.B.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO.	DWG NO. 0103-00-0706 REV D
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

NOTE UNLESS OTHERWISE SPECIFIED



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: DIGIT 1 / MIXER PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO: 172B; DWG NO: 0101-00-0706; REV:
	DO NOT SCALE DWG		CODE IDENT: 23338; SHEET 1 OF 1
	SCALE		

REV	ECN	BY	DATE	APP

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PA
NONE	ASSY DRWG, DIGIT 1	0101-00-0706
NONE	SCHEMATIC, DIGIT 1	0103-00-0706
T1	TRANSFORMER	172-537
L7	COIL, 30MC BPF	172-545
L11	COIL, 35MC BPF	172-546
L12	COIL, 35MC BPF	172-547
L13	COIL, 35MC BPF	172-548
L14	COIL, 35MC BPF	172-549
A1	35/40 MHZ VCO MODULE	172-519
NONE	SHIELD	1400-00-6171
NONE	SHIELD	1400-00-6181
NONE	SHIELD, SYNTH	1400-00-6193
C43 C46 C50	CAP, CER, .001MF, 1KV	DD-102
C18 C20 C25 C26 C27 C32 C34 C40 C41 C44 C45 C47 C51 C54 C8	CAP, CER, MN, .01MF, 50V	CACD2Z5U103Z
C1 C10 C2 C21 C22 C23 C24 C3 C33 C4 C55 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z
C16	CAP, CER, .0022, 1KV	DD-222SLL

WAVETEK PARTS LIST — TITLE: PCA, DIGIT 1 — A 1 — P

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PA
C39	CAP, MICA, 100PF, 500V	DM15-101J
C12 C48	CAP, MICA, 15PF, 500V	DM15-150J
C38 C42	CAP, MICA, 150PF, 500V	DM15-151J
C49 C52 C53	CAP, MICA, 20PF, 500V	DM15-200J
C37	CAP, MICA, 30PF, 500V	DM15-300J
C6	CAP, MICA, 470PF, 500V	DM15-471J
C28 C29 C30 C31	CAP, MICA, 56PF, 500V	DM15-560J
C11	CAP, MYLAR, .01MF, 100V	225P10391WD3
C5	CAP, MLAR, .0047MF100V	225P47291WD3
C13 C14 C15 C17 C19 C35 C36	CAP, TANT, 22MF, 15V	196D226X9015
NONE	1ST DIGIT MIXER BD	1700-00-0706
L1 L2	CHOKE, 1000MIC H, 5%	2500-28
L10 L4 L9	CHOKE, 82MH, 5%	1537-72
L5 L6	CHOKE, 3.3MH, 10%	1537-24
L8	CHOKE, 10MH, 10%	1537-36
L3	CHOKE, 200MH, 5%	1537-90
NONE	SKT, IC, 16PIN	DILB-16P-108

WAVETEK PARTS LIST — TITLE: PCA, DIGIT 1

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TRANS	2N3903	NSC	4901-03-9030	2
IC, MIXER	MD108	ANZAC	7000-01-0800	1
IC	LM 301AN	NSC	7000-03-0100	1
IC	MC1458P1	MOT	7000-14-5800	1
IC	MC1496P	MOT	7000-14-9600	1
IC	7404	TI	8000-74-0400	1
IC	74S10	SIG	8000-74-1001	1
IC	74S74	TI	8000-74-7401	1
IC	MC10125P	MOT	8001-01-2500	1
IC	74LS139	SIG	8007-41-3910	1
IC	74LS175	TI	8007-41-7510	1
IC	74LS196	SIG	8007-41-9610	2
IC	MC4044P	MOT	8100-40-4400	1
IC, SEL, MC10116P QTY: 1: 8001-01-1600	8200-00-0012	WVTK	8200-00-0012	3
IC, PROGRAMMED REF: 8007-41-8801	8600-00-0007	WVTK	8600-00-0007	1

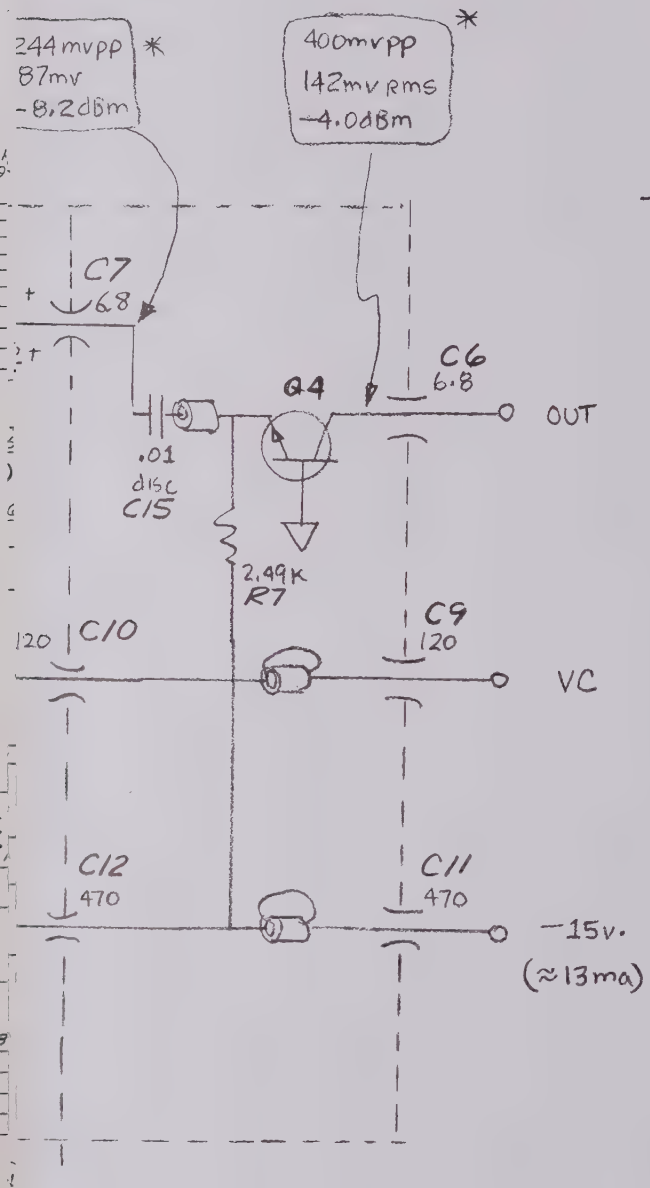
DIGIT 1 — ASSEMBLY NO. 1100-00-0706 — REV F — PAGE: 5

NOTE UNLESS OTHERWISE SPECIFIED

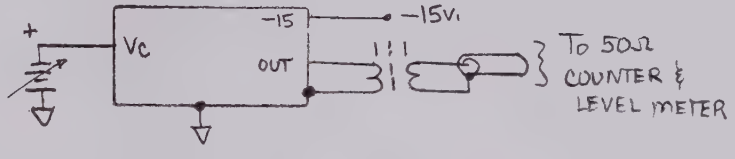
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, DIGIT 1
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 172B — DWG NO 1100-00-0706 — REV F
	SCALE		CODE IDENT 23338 — SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO A 3894

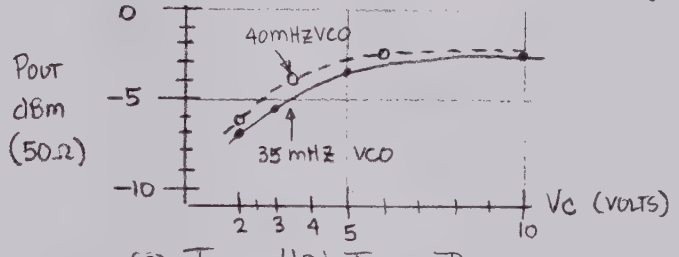
REV	ECN	BY	DATE	APP
A	LOOP2 Added	TVS	18 May	
B	ADD T1, DELETE +5V	✱	26 May	
C	TUNE UP / TEST DATA	TVS	20 JULY	



TUNE UP & TEST DATA



(1) OUTPUT LEVEL VS Vc · (TYPICAL)



(2) TUNE UP & TEST DATA:

	Vc	FOUT	COMMENTS
DIGIT 1 VCO	3.0v.	35 ± 0.1 mHz	TUNE L1 FOR THIS
	5.0v	39.4 ± 0.3	CHECK POINT
	10.0v	47.5 ± 1.5	" "
DIGIT 2 VCO	3.5v.	40. ± 0.1 mHz	TUNE L1 FOR THIS
	6.0v.	45.9 ± 0.35	CHECK POINT
	10v.	53.1 ± 1.5	" "

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN TVS	DATE 16 Apr	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR J. Kolb / TVS	SEP 8 77	TITLE 35/40 mHz VCO MODULE (FOR DIG1 & DIG23 LOOPS)
	RELEASE APPROV	1976	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. / DWG NO. 0104-00-0519 / REV C
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

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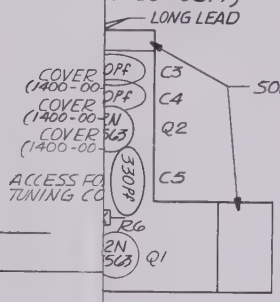
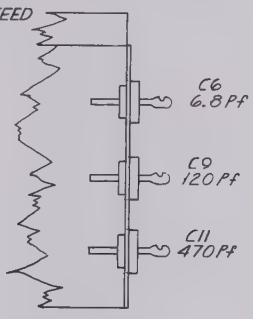
REV	ECN	BY	DATE	APP

RD COMPONENT INSTALL.
00-00-0519)



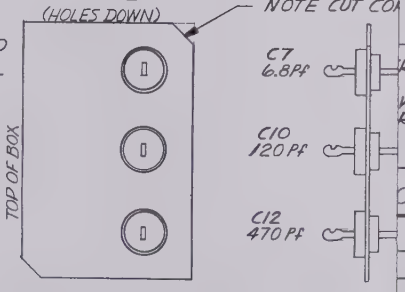
ASSEMBLY SEQUENCE

- **STEP 1** SOLDER CORNERS OF BOX
- **STEP 2** INSTALL FEED THRU CAPACITORS ON BOX

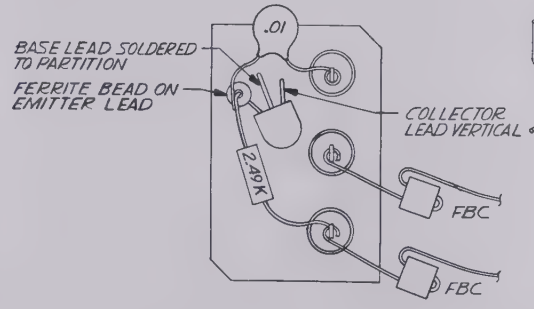


- **STEP 3** INSTALL FEED THRU CAPACITORS ON PARTITION "B"

NOTE:
SEE PARTITION AND COVER DETAIL FOR CAPACITOR ORIENTATION OF THIS PARTITION

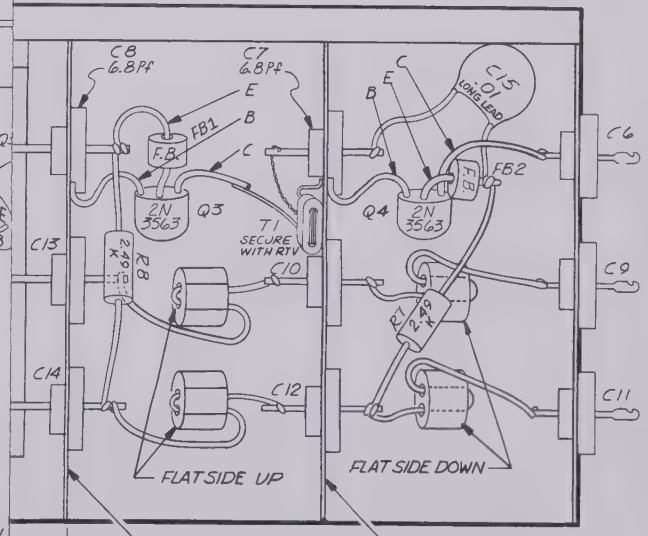


- **STEP 4** INSTALL COMPONENTS ON PARTITION "B"



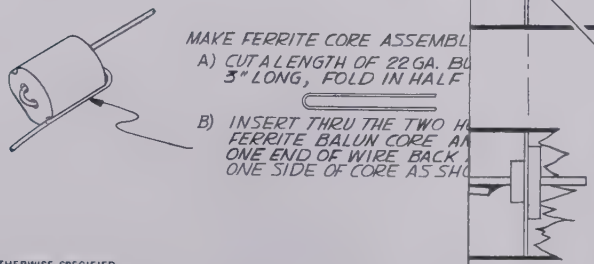
- **STEP 11** INSTALL PARTITION IN BOX USING COVER AS SPACER, JOIN WIRES FROM FIRST PARTITION TO SECOND PARTITION.
- **STEP 12** ASSEMBLE P.C. BOARD.
- **STEP 13** MOUNT COIL IN BOX
- **STEP 14** MOUNT P.C. BOARD IN BOX AND CONNECT TO COIL. NOTE THAT THE P.C. BOARD MUST BE INSTALLED AT ANGLE SHOWN FOR TUNING ACCESS OF COIL

OT SHOWN FOR CLARITY



REF. PARTITION "B" — REF. PARTITION "B"

MAKE FERRITE CORE ASSEMBL
A) CUT A LENGTH OF 22GA. BU
3" LONG, FOLD IN HALF
B) INSERT THRU THE TWO H
FERRITE BALUN CORE AN
ONE END OF WIRE BACK
ONE SIDE OF CORE AS SH



NOTE UNLESS OTHERWISE SPECIFIED

DRAWN D. COOPER	DATE 7-27-76	WAVETEK SAN DIEGO • CALIFORNIA
PROJ ENGR Tom Saliga	DATE Sept 8'77	TITLE ASSEMBLY 35 40 MHz VCO MODULE
RELEASE APPROV		
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
DO NOT SCALE DWG	MODEL NO	DWG NO 0102-00-0519 REV
SCALE	CODE IDENT 23338	SHEET 1 OF 1

0102-00-2000

REV	ECN	BY	DATE	APP

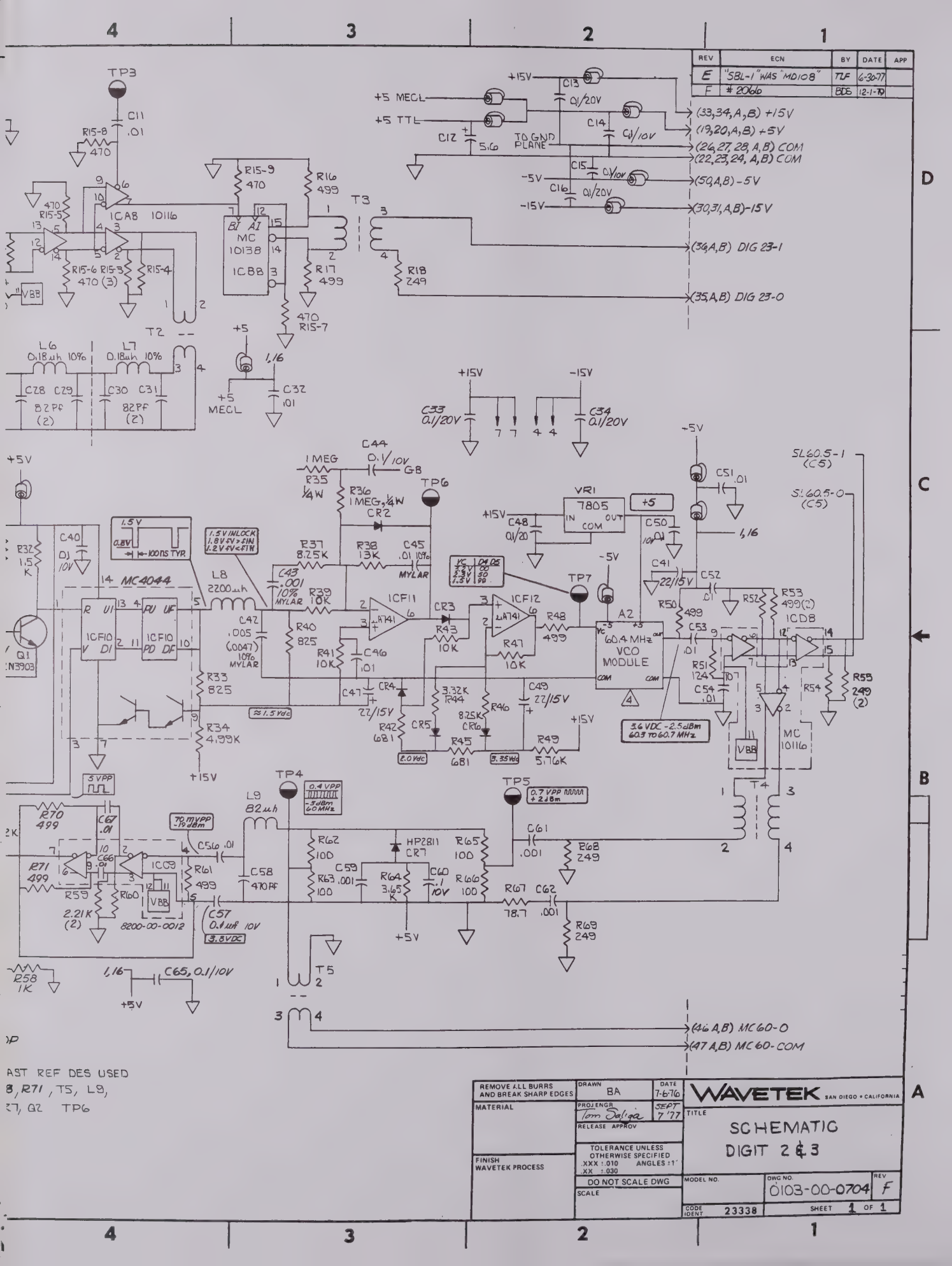
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, VCO MOD	0102-00-0519	WVTK	0102-00-0519	1
NONE	SCHEMATIC, VCO MOD	0104-00-0519	WVTK	0104-00-0519	1
L1	COIL, 35MHZ VCO	172-550	WVTK	1204-00-0550	1
T1	TRANSFORMER	172-551	WVTK	1204-00-0551	1
NONE	PARTITION (B)	1400-00-6081	WVTK	1400-00-6081	2
NONE	COVER (C)	1400-00-6101	WVTK	1400-00-6101	1
NONE	COVER (B)	1400-00-6111	WVTK	1400-00-6111	2
NONE	BOX, OSCILLATOR	1400-00-6141	WVTK	1400-00-6141	1
C1 C2	CAP, CER, .001MF, 1KV	DD-102 LONG LEAD	CRL	1500-01-0201	2
C15	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
C3 C4	CAP, CER, 30PF, 1KV	DD-300	CRL	1500-03-0001	2
C5	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	1
C10 C9	CAP, FTHRU, 120PF, 500V	54-794-005-X5R0-121K	SPECT	1500-61-2106	2
C11 C12 C13 C14	CAP, FTHRU, 470PF, 500V	54-794-010-X5R0-471M	SPECT	1500-64-7106	4
C6 C7 C8	CAP, FTHRU, 6.8PF, 500V	54-794-010-X5E0-689M	SPECT	1500-66-8906	3
NONE	VCO MOD	1700-00-0519	WVTK	1700-00-0519	1
FB1 FB2	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	2
NONE	BALUN CORE	2873000902	FARIT	3100-00-0002	4

WAVETEK PARTS LIST	TITLE 35/40 MHZ VCO MODULE	ASSEMBLY NO. 1206-00-0519 PAGE: 1	REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R4	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	1
R3 R6	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	2
R7 R8	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	2
R5	RES, MF, 1.8W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	1
R1 R2	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	2
CR1	DIODE	141	ITT	4803-02-0141	1
Q1 Q2 Q3 Q4	TRANS	2N3563	FAIR	4901-03-3630	4

WAVETEK PARTS LIST	TITLE 35/40 MHZ VCO MODULE	ASSEMBLY NO. 1206-00-0519 PAGE: 2	REV A

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST 35/40 MHZ VCO MODULE
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 172B / DWG NO 1206-00-0519 / REV A
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		


REV | ECN | BY | DATE | APP
E | "SBL-1" WAS "MD108" | TLF | 6-30-77
F | # 2066 | BDS | 12-1-77
TP3
C11 .01
R15-8 470
ICA8 10116
R15-9 470
R16 499
R17 499
R18 249
T3
T2
L6 0.18µh 10%
L7 0.18µh 10%
C28 C29 82PF (2)
C30 C31 82PF (2)
R15-6 R15-3 470 (3)
R15-4
R15-5 470
R15-7 470
+15V
-15V
+5 MECL
+5 TTL
TO GND PLANE
C13 .01/20V
C14 .1/10V
C15 .1/10V
C16 .01/20V
C12 5.6
(33,34,A,B) +15V
(19,20,A,B) +5V
(24,27,28,A,B) COM
(22,23,24,A,B) COM
(50,A,B) -5V
(30,31,A,B) -15V
(36,A,B) DIG 23-1
(35,A,B) DIG 23-0
C32 .01
1/16
C33 0.1/20V
C34 0.1/20V
C44 0.1/10V
1 MEG R35 1/4W
R36 1 MEG, 1/4W
CR2
TP6
VR1 7805
C48 .01/20
C50 .01
C51 .01
C41 22/15V
C52 .01
TP7
A2 60.4 MHz VCO MODULE
3.6 VDC -2.5dBm 60.3 TO 60.7 MHz
R50 499
R51 124
R52
R53 499(2)
R54
R55 249 (2)
C53 .01
C54 .01
MC 10116
SL60.5-1 (C5)
SL60.5-0 (C5)
1.5V
0.8V
100 NS TYP
1.5V INLOCK
1.8V 4V > ±IN
1.2V 4V < ±IN
14 MC4044
ICF10 V DI
ICF10 PD DF
Q1 2N3903
L8 2200µh
C43 .001 10% MYLAR
C42 .005 (.0047) 10% MYLAR
R37 8.25K
R38 13K
C45 .01 10% MYLAR
R39 10K
R40 825
R41 10K
C46 .01
ICF11 µA741
ICF12 µA741
CR3
R43 10K
R47 10K
R48 499
C47 22/15V
CR4
CR5
CR6
R42 681
R44 3.32K
R46 8.25K
R45 681
C49 22/15V
R49 5.76K
R33 825
R34 4.99K
≈1.5 Vdc
2.0 Vdc
5.35 Vdc
5 VPP
0.4 VPP -3dBm 60 MHz
0.7 VPP +21dBm
70 mVPP -7dBm
TP4
TP5
L9 82µh
T4
T5
R70 499
C67 .01
R71 499
C66 .01
C56 .01
ICC9
R61 499
R59 2.21K (2)
R60
C58 470PF
C57 0.1µf 10V
3.8VDC
8200-00-0012
R62 100
R63 100
C59 .001
HP2811 CR7
R64 3.65K
C60 1 10V
R65 100
R66 100
C61 .001
R67 78.7
C62 .001
R68 249
R69 249
R58 1K
C65, 0.1/10V
(46 A,B) MC60-0
(47 A,B) MC60-COM
AST REF DES USED
8, R71, T5, L9,
27, Q2 TP6
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN BA DATE 7-6-76
PROJ ENGR Tom Saliga SEPT 7'77
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC DIGIT 2 & 3
MODEL NO.
DWG NO. 0103-00-0704 REV F
CODE IDENT 23338
SHEET 1 OF 1

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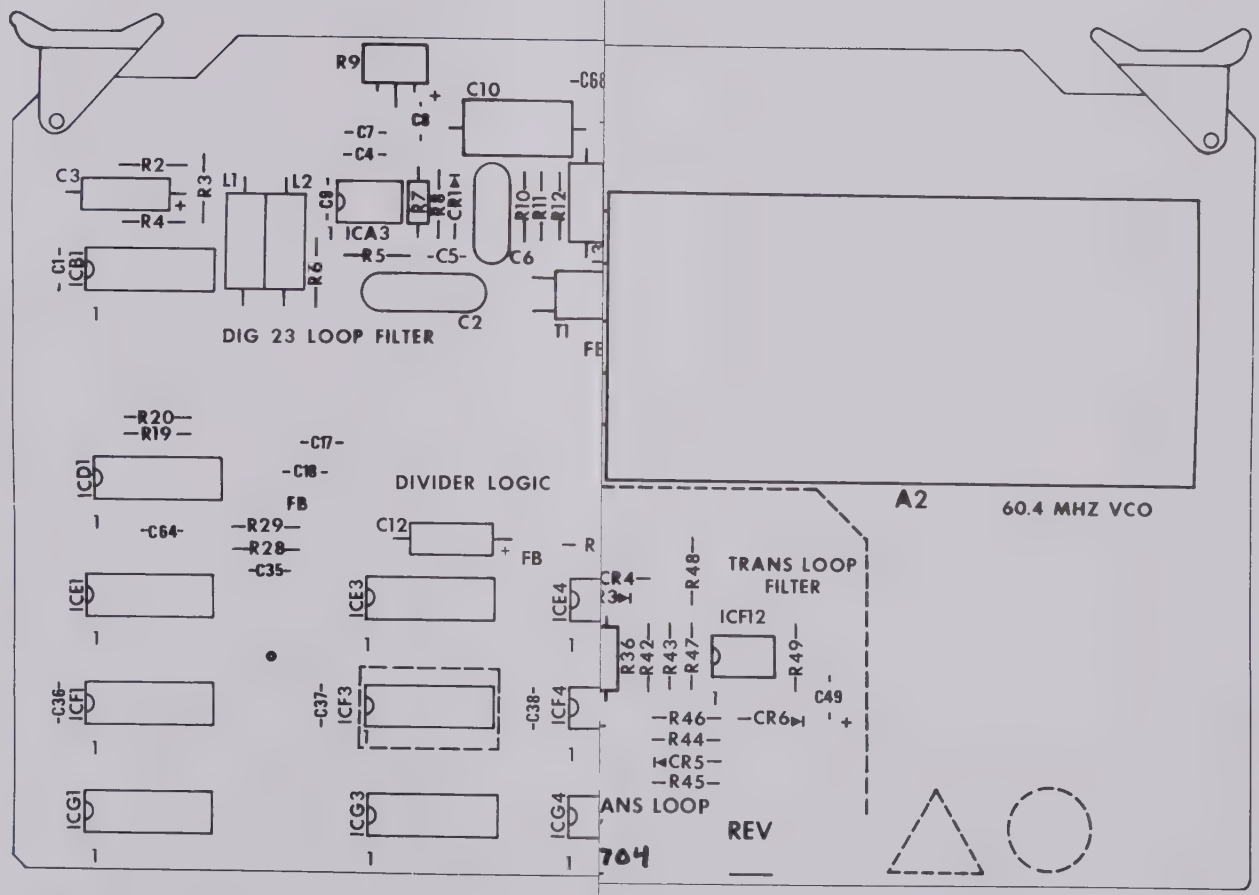


11DD-00-0704

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: DIGITS 2 & 3 PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG		MODEL NO 172B; DWG NO 0101-00-0704; REV
	SCALE		CODE IDENT 23338; SHEET 1 OF 1

REV	ECN	BY	DATE	APP

IG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
182-2	AMP	2100-05-0020	1
5368-3C-5A	UNICP	2800-05-6114	5
3 RED	CALMK	2800-07-0010	2
123N	METRS	2800-11-0003	14
73000902	FARIT	3100-00-0002	14
AR2K	BECK	4600-02-0201	1
20GF-155	STKPL	4700-25-1504	1
55D-1000F	TRW	4701-03-1000	8
55D-1001F	TRW	4701-03-1001	3
55D-1002F	TRW	4701-03-1002	6
55D-1240F	TRW	4701-03-1240	1
55D-1302F	TRW	4701-03-1302	1
55D-1500F	TRW	4701-03-1500	3
55D-1501F	TRW	4701-03-1501	2
55D-2001F	TRW	4701-03-2001	1
55D-2211F	TRW	4701-03-2211	2
55D-2490F	TRW	4701-03-2490	6

ASSEMBLY NO.	REV
1100-00-0704	J
PAGE: 3	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR1 CR2 CR3 CR4 CR5 CR6	DIODE	1N4148	FAIR	4807-02-6666	6
CR7	DIODE	5082-2811	HP	4809-02-2811	1
Q1 Q2	TRANS	2N3903	NSC	4901-03-9030	2
ICD6	IC, MIXER	MD108	ANZAC	7000-01-0800	1
ICA3	IC	LM 301AN	NSC	7000-03-0100	1
ICF11 ICF12	IC	LM741CN	NSC	7000-07-4100	2
ICF1	IC	74S02	SIG	8000-74-0201	1
ICE1	IC	7474	TI	8000-74-7400	1
VR1	VOLTAGE REGULATOR	MA7805UC	FAIR	8000-78-0500	1
ICD1	IC	MC10125P	MOT	8001-01-2500	1
ICB8	IC	MC10138P	MOT	8001-01-3800	1
ICG4	IC	74LS139	SIG	8007-41-3910	1
ICG1	IC	74S140	TI	8007-41-4001	1
ICE4 ICF4	IC	74LS175	TI	8007-41-7510	2
ICE3 ICF3 ICG3	IC	74LS192	TI	8007-41-9210	3
ICB1 ICF10	IC	MC4044P	MOT	8100-40-4400	2
ICA8 ICC9 ICD5 ICD8	IC, SEL, MC10116P	8200-00-0012	WVTK	8200-00-0012	4

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, 2ND DIGIT TRANS	1100-00-0704	J
		PAGE: 5	

IG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
55D-2740F	TRW	4701-03-2740	1
55D-3321F	TRW	4701-03-3321	1
55D-3322F	TRW	4701-03-3322	2
55D-33R2F	TRW	4701-03-3329	1
55D-3651F	TRW	4701-03-3651	1
55D-4642F	TRW	4701-03-4642	1
55D-4990F	TRW	4701-03-4990	13
55D-4991F	TRW	4701-03-4991	2
55D-51R1F	TRW	4701-03-5119	1
55D-5761F	TRW	4701-03-5761	1
55D-6810F	TRW	4701-03-6810	3
55D-78R7F	TRW	4701-03-7879	1
55D-8250F	TRW	4701-03-8250	2
55D-8251F	TRW	4701-03-8251	2
0D-1004F	TRW	4701-13-1004	2
0R-101-471	BOURN	4770-00-0009	2

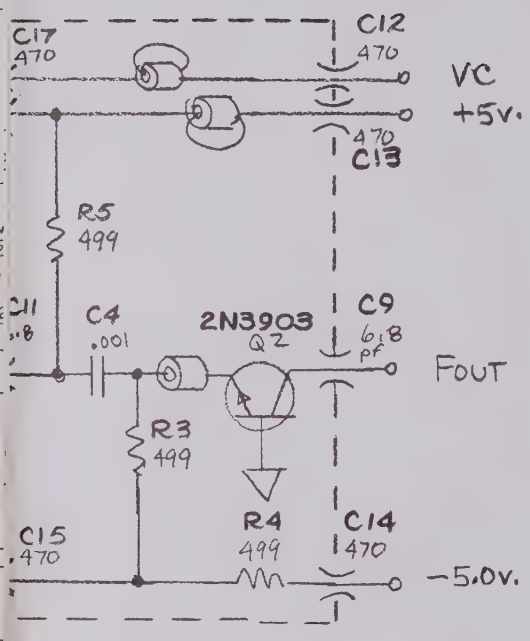
ASSEMBLY NO.	REV
1100-00-0704	J
PAGE: 4	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	QTY: 1: 8001-01-1600				

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, 2ND DIGIT TRANS	1100-00-0704	J
		PAGE: 6	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, 2ND DIGIT TRANS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 172B	DWG NO 1100-00-0704 REV J
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	Piston Trimmer moved	TVS	June 76	TVS
B	CHANGED: C2 FROM .001 TO 910	DC	22377	TVS



470pf fdthru: 10
6.8pf " 3

-Vcc correction : 24Feb

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN T.V. Saliga	DATE 16 Feb	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR T. V. Saliga	SEPT 8 '77	TITLE 60.4 MHz VCO MODULE FOR SUM LOOP	
	RELEASE APPROV			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030			
	DO NOT SCALE DWG		MODEL NO.	DWG NO. 0103-00-0520 REV B
	SCALE		CODE IDENT 23338	SHEET 1 OF 1

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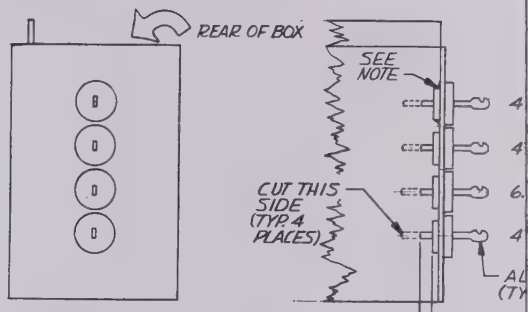
ASSEMBLY SEQUENCE

- STEP 1 SOLDER CORNERS OF BOX

STEP 2 STAND BOX ON END WITH WEIGHT. IN
THRU CAPACITORS AND ALIGN TERMINALS ON CAPACI
SAME DIRECTION AS SHOWN.



NOTE: SOLDER SO THAT CAPACITOR IS SOLDERED TO BOX ALL AROUND THE ENTIRE CAPACITOR BODY.

PARTITION "A"

N "A" INTO BOX
AS A SPACER

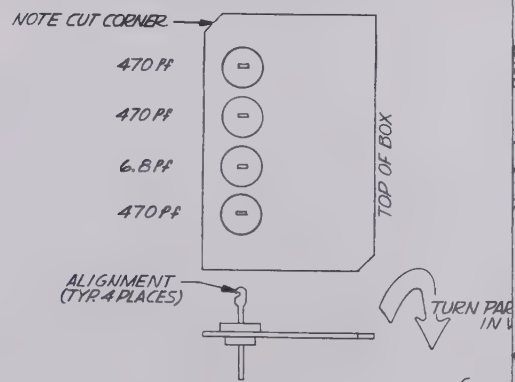
E COMPARTMENT
PER SAMPLE.

RE VERY FRAGILE
5/16" OPEN END
CAPACITOR WITH
ON FLATTENED
OP IN WIRE FROM
REVENT STRAIN

NOT BLOCK
8 Pf CAP.

ICA

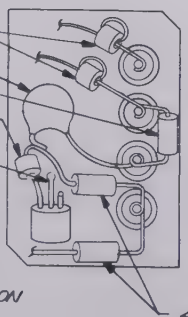
- STEP 3 HOLD CORNER OF PARTITION "C" IN BEN
INSTALL FEED THRU CAPACITORS AND ALIGN TERMIN



N SLEEVING

COIL TAP IN
COMPARTMENT

FOR
TRANSI
LEAD TO
EMITTER 3/16
BODY TO ALL
FOR FERRITE
ISTOR CLEARA

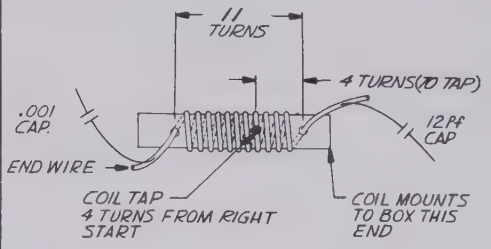


- INSTALL FERRITE BEADS 2
- INSTALL .001 CAP
- INSTALL 499Ω RESISTOR
- INSTALL FERRITE BEAD ON EMITTER LEAD
- SOLDER 2N3903 TO PARTITION SO TRANSISTOR BOTTOM IS EVEN WITH END CAP CENTER POST

NOTE: AT THIS POINT THE COLLECTOR LEAD IS UNUSED AND REMAINS IN A VERTICAL POSITION

499Ω RESISTO

NOTE UNLESS OTHERWISE SPECIFIED



COIL DETAIL

NOTE: USE 20GA. WIRE AND COAT COIL WIRE WITH POLYSTYRINE Q-DOPE

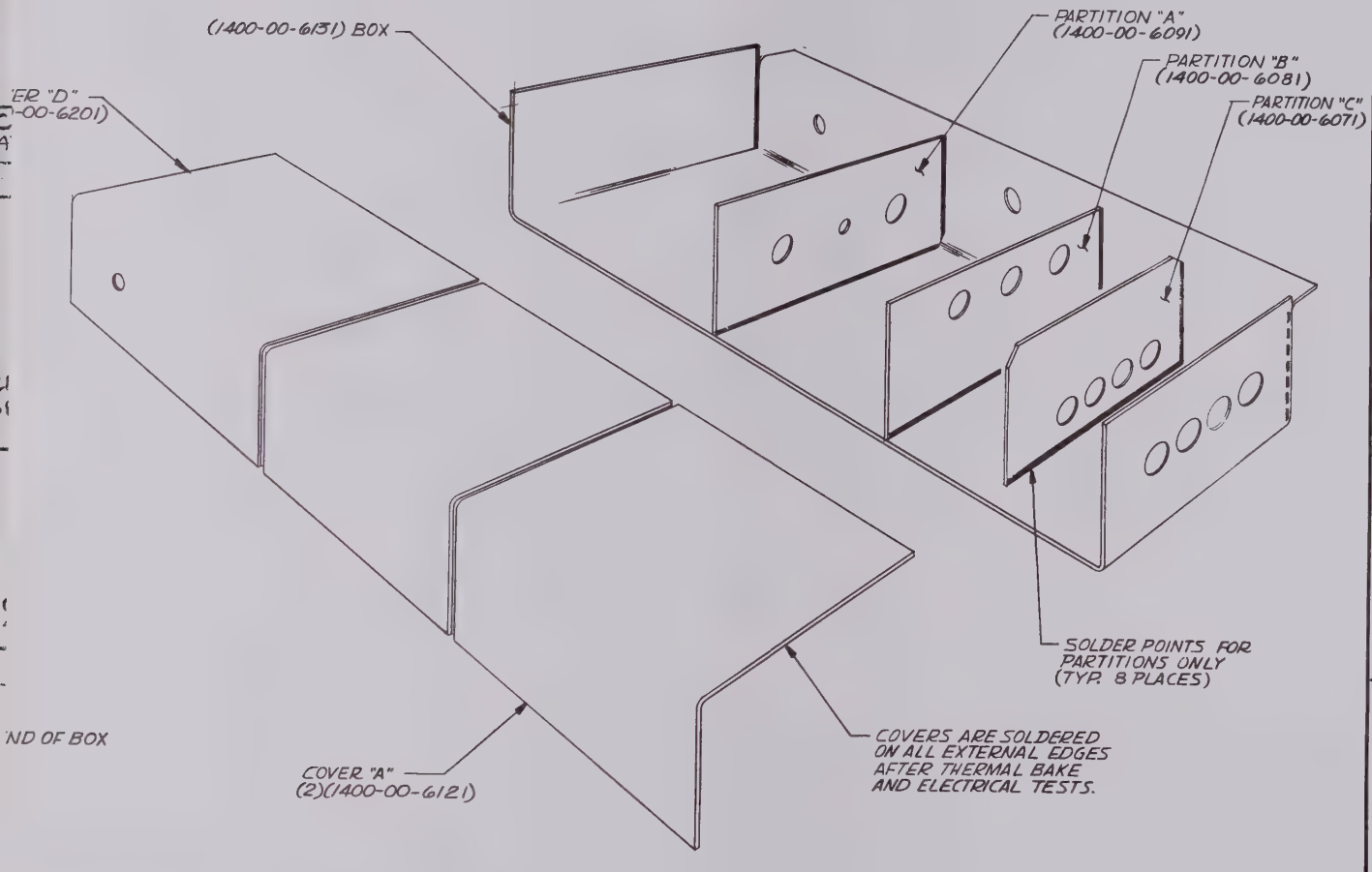
REV	ECN	BY	DATE	APP
C	ECN 1693 & 1687	RO	3/13/78	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 7-29-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR T. Selga	SEPT 8'77	TITLE ASSEMBLY 60.4 MHz VCO MODULE, DIGITS 2 AND 3
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1° XX : 030		MODEL NO.
	DO NOT SCALE DWG		DWG NO. 0102-00-0520 REV C
	SCALE		CODE IDENT 23338 SHEET 1 OF 2

0102-00-0520

REV	ECN	BY	DATE	APP

PARTITIONS AND COVERS INSTALLATION


(1400-00-6131) BOX
PARTITION "A" (1400-00-6091)
PARTITION "B" (1400-00-6081)
PARTITION "C" (1400-00-6071)
ER "D" -00-6201)
SOLDER POINTS FOR PARTITIONS ONLY (TYP. 8 PLACES)
ND OF BOX
COVER "A" (2)(1400-00-6121)
COVERS ARE SOLDERED ON ALL EXTERNAL EDGES AFTER THERMAL BAKE AND ELECTRICAL TESTS.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 7-30-76	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Tom Saliga	DATE SEPT 8'77	TITLE ASSEMBLY 60.4 MHz VCO MODULE, DIGITS 2 AND 3
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		MODEL NO
	DO NOT SCALE DWG		DWG NO. 0102-00-0520 REV C
	SCALE		CODE IDENT 23338 SHEET 2 OF 2

0102-00-0520

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REV	ECN	BY	DATE	APP

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
ASSY DRWG, VCO MOD	0102-00-00520	WVTK	0102-00-0520	1
SCHEMATIC, VCO MOD	0103-00-0520	WVTK	0103-00-0520	1
INDUCTOR, 60.4MHZ	172-604	WVTK	1204-00-0604	4
PARTITION "C"	1400-00-6071	WVTK	1400-00-6071	1
PARTITION (B)	1400-00-6081	WVTK	1400-00-6081	1
PARTITION (A)	1400-00-6091	WVTK	1400-00-6091	1
COVER (A)	1400-00-6121	WVTK	1400-00-6121	2
BOX, OSCILLATOR	1400-00-6131	WVTK	1400-00-6131	1
COIL FORM	1400-00-6150	WVTK	1400-00-6150	1
COVER (D)	1400-00-6201	WVTK	1400-00-6201	1
CAP, CER, .001MF, 1KV	DD-102 LONG LEAD	CRL	1500-01-0201	2
CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
CAP, MICA, 12PF, 500V	DM15-120J	ARCO	1500-11-2000	1
CAP, MICA, 68PF, 500V	DM15-680J	ARCO	1500-16-8000	1
CAP, 910PF, 100V, 1%	DM15-911F	ARCO	1500-19-1101	1
CAP, PISTON TRIMMER	GSG146	SPRGD	1500-50-9000	1
CAP, FTHRU, 470PF, 500V	54-794-010-X5R0-471M	SPECT	1500-64-7106	10

MHZ VCO MOD	ASSEMBLY NO 1206-00-0520 PAGE: 1	REV C

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CAP, FTHRU, 6.8PF, 500V	54-794-010-X5E0-689M	SPECT	1500-66-8906	3
CAP, CER, .1MF, 50V	DG45BX104MP	WSTCP	1509-90-0011	1
60.4MHZ VCO MODULE	1700-00-0520	WVTK	1700-00-0520	1
FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	3
RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	1
RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	5
DIODE	141	ITT	4803-02-0141	1
TRANS	2N3903	NSC	4901-03-9030	2
IC	MC1648P	MOT	8100-16-4810	1

MHZ VCO MOD	ASSEMBLY NO. 1206-00-0520 PAGE 2	REV C

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

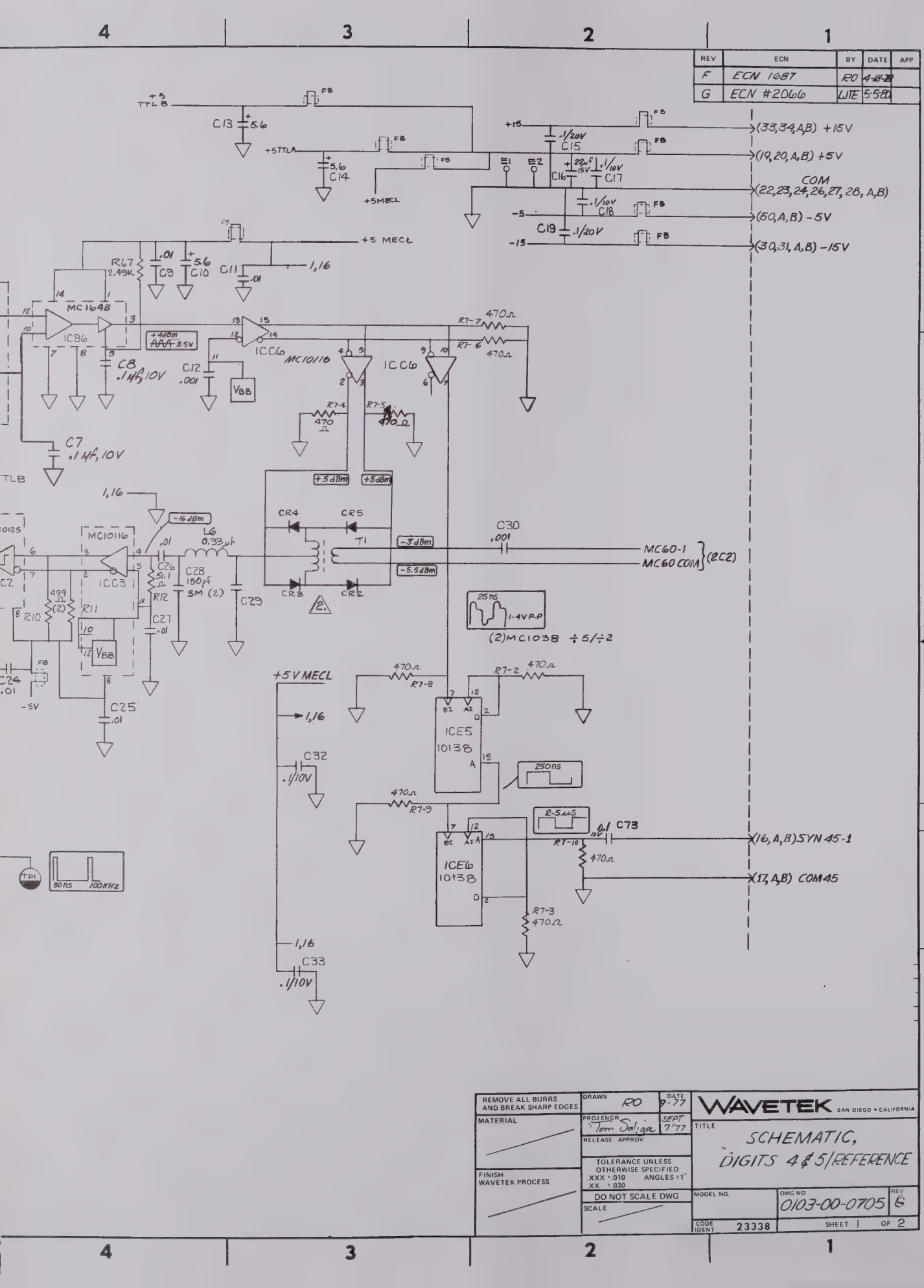
PARTS LIST
60.4 MHZ VCO MOD

MODEL NO	DWG NO	REV
172B	1206-00-0520	C

CODE IDENT 23338 SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

B SHOP GRAPHICS/ACCUPRESS REORDER NO A 3894


4
3
2
1
REV | ECN | BY | DATE | APP
F | ECN 1687 | RO | 4-18-78
G | ECN #2066 | LITE | 5-5-80
D
C
B
A
+5 TTL B
+5TTLA
+5MECL
+5 MECL
+15
-5
-15
C13 5.6
C14 5.6
C15 .1/20V
C16 22µf 15V
C17 .1/10V
C18 .1/10V
C19 .1/20V
FB
E1
E2
(33,34,A,B) +15V
(19,20,A,B) +5V
COM
(22,23,24,26,27,28, A,B)
(50,A,B) -5V
(30,31,A,B) -15V
R67 2.49K
C9 .01
C10 5.6
C11 .01
1,16
MC1648
ICB6
+4dBm
3.5V
C8 .1MF, 10V
C12 .001
VBB
ICC6
MC10116
R7-7 470Ω
R7-6 470Ω
R7-4 470Ω
R7-5 470Ω
C7 .1MF, 10V
TTLB
+5dBm
+5dBm
-16dBm
MC10116
ICC3
L6 0.33µh
C26 51.1Ω
C28 150pf SM (2)
C29
R12
R11
499 (2)
R10
C27 .01
C24 .01
C25 .01
-5V
CR4
CR5
T1
CR3
CR2
-3dBm
-5.5dBm
C30 .001
MC60-1
MC60 COM
(2C2)
25ns
1-4V P-P
(2)MC1038 ÷5/÷2
+5V MECL
470Ω
R7-8
R7-2
ICE5
10138
250ns
R7-9
2-5µs
C73 .01
R7-10
ICE6
10138
R7-3 470Ω
(16,A,B) SYN 45-1
(17,A,B) COM45
C32 .1/10V
C33 .1/10V
TP1
80ns
100KHz
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN RO DATE 9-77
PROJ ENGR Tom Saliga SEPT 7'77
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC, DIGITS 4 & 5/REFERENCE
MODEL NO.
DWG NO 0103-00-0705
REV G
CODE IDENT 23338
SHEET 1 OF 2

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REV	ECN	BY	DATE	APP

+5V TTLA P.1
+15V P.1
-15V P.1

9 ± 1.5 dBM 60MHz.

REF/OSC & VCXO

CRYST GLUED INSULTD PCB
XTL 1
14T
L2
39pf SM 5%
C34
C35 68PF, 5% SM
49.9K R13
C37 82 pf SM 5%
.001 C36
CR9 MV2109
VC10 B1
VCGRD-A2
-1.15 VDC
R14 2.21K
C55 499Ω R 32
470Ω R23-8
C56 .01
ICA12
R23-9 470Ω
78.7Ω R21
.5VP-P
MC60COM (47A,B)
MC60-Ø (46A,B)
MC60-1 (1C2)
MC60-COM (1C2)
MC30-0 (38A,B)
MC30-1 (39AB)
51.1Ω R34
INT 10 (43AB) REF OUT
ICF11 D11
MC0.1 (1D7)
MC0.1 (21 A,B)
MC0.5 (18A)
MCCOM (18B)
C60 .01
CR18
+5 TTLA
SYNPR-Ø (14B) [CI2]
CR10
REF IN (29AB) EXT CLK 10MHz (1VRMS)
±3PPM
.01 C57
R35 1K
R36 2K
C61 .01
10pf C58
C59 .01
33.2K R37
CR11
C62 .1/10V
R65 1.5K
VC10 (C8)
2.4VDC
R64 38.2K
3.2K R62
6.19K R63
5.6 C72
LOCK-Ø (15B) [CI1]
CAUTION-Ø (15A) [CIØ]
+15V 150K R38
VCGRD. C8
E5
E6

8. USE FERRITE BEAD NO. 3100-00-0002.
7. ALL .001, .01 & .1 CAPS ARE CERAMIC DISC.
6. DIODES UNMARKED ARE FD6666
5. XTL 1: 10:00 MHz CRYSTAL PER SPEC.
4. VC10 JUMPERS TO ITSELF ON SAME PCB; @ T.P. : -0.4v T

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS

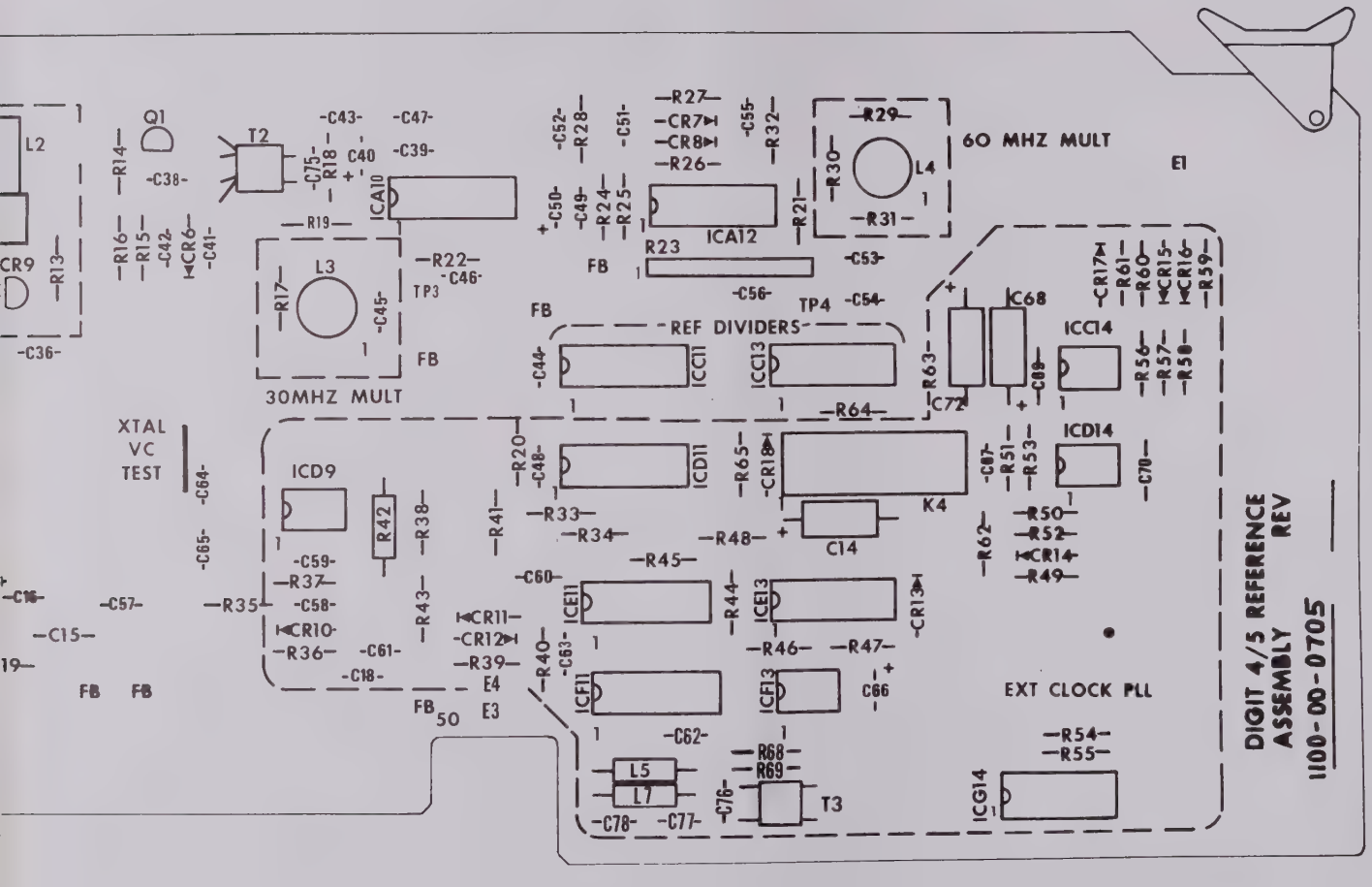
DRAWN RO DATE 6 11-76
PROJ ENGR Tom Sallee SEPT 7'77
RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± 010 ANGLES ± 1°
XX ± 030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC,
DIGITS 4&5/REFERENCE

MODEL NO.
DWG NO. 0103-00-0705 REV G
CODE IDENT 23338
SHEET 2 OF 2



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: DIGITS 4&5/REF PCA
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ·010 ANGLES ·1; XX ·030		MODEL NO: 1726
	DO NOT SCALE DWG		DWG NO: 0101-00-0705
	SCALE		REV
			CODE IDENT 23338
			SHEET 1 OF 1

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PAR
NONE	ASSY DRWG, DIGIT 4&5	0101-00-0705
NONE	SCHEMATIC, DIGIT 4-5	0103-00-0705
T1	TRANSFORMER MIXER	172-538
T2	TRANSFORMER	172-540
L1	COIL, 40MC VCO	172-541
L3	COIL, 30MC MULT	172-543
L4	COIL, 60MC MULT	172-544
L2	COIL, XTAL TUNE	1204-00-0627
NONE	SHIELD, SYNTH	1400-00-6193
NONE	SHIELD, OSC	1400-00-6631
C58	CAP, CER, 10PF, 1KV	DD-100LL
C12 C30 C36 C55	CAP, CER, .001MF, 1KV	DD-102 LONG L
C1 C11 C2 C24 C25 C26 C27 C31 C41 C42 C43 C44 C47 C48 C49 C5 C52 C56 C57 C59 C60 C61 C63 C64 C65 C67 C74 C9	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z1
C15 C17 C18 C19 C20 C21 C22 C23 C32 C33 C39 C62 C69 C7 C70	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z0

WAVETEK PARTS LIST	TITLE PCA, DIGIT 4-5	AS 11 PA

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PAR
C73 C8		
C51	CAP, CER, 15PF, 1KV	DD-150
C46	CAP, MICA, 100PF, 500V	DM15-101J
C53	CAP, MICA, 15PF, 500V	DM15-150J
C28 C29 C6	CAP, MICA, 150PF, 500V	DM15-151J
C45	CAP, MICA, 30PF, 500V	DM15-300J
C34 C38	CAP, MICA, 39PF, 500V	DM15-390J
C75T	CAP, MICA, 56PF, 500V	DM15-560J
C37	CAP, MICA, 68PF, 500V	DM15-680J
C35 C54	CAP, MICA, 82PF, 500V	DM15-820J
C3	CAP, MYLAR, .022MF100V	225P22391WD3
C16 C40 C50 C66	CAP, TANT, 22MF, 15V	196D226X9015H
C10 C13 C14 C4 C68 C72	CAP, TANT, 5.6MF, 35V	150D565X9035B
NONE	4TH/5TH FREQ REF BD	1700-00-0705
L5	CHOKE, 82MH, 5%	1537-72
L6	CHOKE, .33MH, 5%	1537-04
NONE	SKT, IC, 16PIN	DILB-16P-108

WAVETEK PARTS LIST	TITLE PCA, DIGIT 4-5	AS 11 PA

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RES MODULE	4310R-101-471	BOURN	4770-00-0009	2
DIODE	141	ITT	4803-02-0141	1
DIODE	MV2109	MOT	4803-02-2109	1
DIODE	1N4148	FAIR	4807-02-6666	11
DIODE	5082-2811	HP	4809-02-2811	2
DIODE, SET, 5082-2811 QTY: 4: 4809-02-2811	4898-00-0012	WVTK	4898-00-0012	1
TRANS	2N3903	NSC	4901-03-9030	1
IC	NE555V	SIG	7000-05-5500	1
IC	LM741CN	NSC	7000-07-4100	4
IC	74S02	SIG	8000-74-0201	1
IC	7404	TI	8000-74-0400	1
IC	7438	TI	8000-74-3800	1
IC	7474	TI	8000-74-7400	1
IC	74LS74	TI	8000-74-7410	1
IC	7486	TI	8000-74-8600	1
IC	MC10125P	MOT	8001-01-2500	1

IGIT 4-5	ASSEMBLY NO. 1100-00-0705 PAGE: 5	REV E

PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
IC	MC10138P	MOT	8001-01-3800	2
IC	74LS139	SIG	8007-41-3910	1
IC	74S140	TI	8007-41-4001	1
IC	74LS175	TI	8007-41-7510	2
IC	74LS192	TI	8007-41-9210	3
IC	74LS290	TI	8007-42-9010	2
IC	MC1648P	MOT	8100-16-4810	1
IC	MC4044P	MOT	8100-40-4400	1
IC, SEL, MC10116P QTY: 1: 8001-01-1600	8200-00-0012	WVTK	8200-00-0012	5

IGIT 4-5	ASSEMBLY NO. 1100-00-0705 PAGE: 6	REV E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST PCA, DIGIT 4-5
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 172B / DWG NO 1100-00-0705 / REV E
	SCALE		SIZE A / CAGE CODE 23338 / SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS ACCUPRESS REORDER NO. A 3494

Table A-1. American Standard Code for Information Interchange (ASCII)

b7 / b6 / b5 / BITS					0_0	MSG[1]	0_1	MSG	$0_1{}_0$	MSG	$0_1{}_1$	MSG	$1_0{}_0$	MSG	$1_0{}_1$	MSG	$1_1{}_0$	MSG	$1_1{}_1$	MSG
b4	b3	b2	b1	column / row	0		1		2		3		4		5		6		7	
0	0	0	0	0	NUL		DLE		SP	MLA ASSIGNED TO DEVICE	0	MLA ASSIGNED TO DEVICE	@	MTA ASSIGNED TO DEVICE	P	MTA ASSIGNED TO DEVICE	\	MEANING DEFINED BY PCG CODE	p	MEANING DEFINED BY PCG CODE
0	0	0	1	1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2	STX		DC2		"		2		B		R		b		r	
0	0	1	1	3	ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6	ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7	BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10	LF		SUB		*		:		J		Z		j		z	
1	0	1	1	11	VT		ESC		+		;		K		[		k		{	
1	1	0	0	12	FF		FS		,		<		L		\		l		|	
1	1	0	1	13	CR		GS		-		=		M		]		m		}	
1	1	1	0	14	SO		RS		.		>		N		^		n		~	
1	1	1	1	15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

LISTEN ADDRESS GROUP (LAG)[4]

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B

Table B-1. Programming Command Summary

Control and Data Names	Model 172B Key	ASCII Character
Clear Entry	CLR	None
Activate Keyboard	LOCAL	None
Invert and minus	+/–	—
Decimal point	.	.
0	0	0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
Amplitude	AMPL	A
Operating mode	MODE	B
Function (waveform)	FUNC	C
Reference offset	OFST	D
×10 multiplier	EXP	E
Frequency	FREQ	F
Bus address status	ADR	G
Execute	EXEC	I
Trigger	TRIG	J
GET mode	GET	O
50Ω load condition	OUTP	P
Recall commands	CMD RCL	R
Symmetry	SYM	S
Amplitude definition	AMPL DEF	V
Display	(None)	'
Talk response	TLK	T
Previous setting	LAST	U
End of string	TRM	X
Service request	SRQ	Q
Store setting	STOR	M
Recall setting	RCL	Y
Next setting	NEXT	W
Recall fast	(None)	Z

Number of Significant Digits	
Frequency	5 floating (6 when overranging, 10 MHz)
Amplitude	3 floating (4 when overranging, 10V p-p)
Offset	3 floating
All other	1 floating

SRQ (Q) Code	
Off	0
Enabled	1

Function (C) Codes	
Sine	0
Triangle	1
Square	2
None	3
DC	4
+ Pulse	6
– Pulse	7

Mode (B) Codes	
Continuous	0
Triggered	1
Gated	2
Synthesized	3
Triggered haverwave	4
Gated haverwave	5
External phase lock	6

Output Load (P) Codes	
Load out, output on	0
Load in, output on	1
Load out, output off	2
Load in, output off	3

Symmetry (S) Codes	
50%	0 or 5
10% thru 90%	1 thru 9

GET (O) Codes	
Execute and trigger	0
Go to next program, execute and trigger	+1
Go to previous program, execute and trigger	–1

Ampl Def (V) Codes	
V p-p into 50Ω	0
Vrms	1
dBm into 50Ω	2

Talk (T) Codes	
Status	0
Error status	1
SRQ reason	2
Last setting	4

APPENDIX C

Table C-1. 172B Programming Examples

In the following examples, the 172B GPIB address switches are set to 00001. Therefore, the 172B's address on the HP 9825 calculator is 701 (the 7 selects the GPIB interface card, and the 01 selects the 172B). Also, the 172B's address on the HP 9830 calculator is then "!" (Listen address, ASCII exclamation point) or "A" (Talk address, ASCII letter A). Send CMD "?U!" to write; CMD "?A5" to read.

Example 1. Sweep amplitude from 1 to 11 volts in 10 millivolt steps.

Program for the HP 9825 (HPL Language).

Program	Remarks
0: wrt 701,"D0F1E4B0C1P1S3"	Set up other 172B waveform parameters: 0 volts offset, 10 kHz frequency, continuous mode, triangle waveshape, load and output connected, and 30% symmetry. Note that since the Execute action (designated by the letter "I") is not programmed, this information is not yet programmed into the waveform generator circuits. This will happen when the first amplitude is programmed.
1: 1→A	The variable A will be used to hold the current value of the amplitude being sent to the instrument.
2: wrt 701,"A",A,"I"	Send amplitude value to 172B. This is done by sending first the ASCII letter A, then the amplitude in variable A, followed by the letter I, which causes the Execute action, that transfers the information programmed since the last Execute was sent to the waveform generator circuits.
3: A+.01→A	Increment amplitude variable by 10 millivolts.
4: if A<=11;gto 2	Test if value of amplitude variable is less than or equal to 11 volts. If so, go back to statement 2 and send another amplitude. If not, proceed to statement 5.
5: stp	Stop program.

Program for the HP 9830 (BASIC Language).

1000 CMD"?U!","D0F1E4B0C1P1S3"	Set up other 172B waveform parameters: 0 volts offset, 10 kHz frequency, continuous mode, triangle waveshape, load and output connected and 30% symmetry. Note that since the Execute action (designated by the letter "I") is not programmed, this information is not yet programmed into the waveform generator circuits. This will happen when the first amplitude is programmed.
1010 FOR A = 1 TO 11 STEP .01	The variable A will be used to hold the current value of the amplitude being sent to the instrument.

Table C-1. 172B Programming Examples (Continued)

Example 1. Sweep Amplitude from 1 to 11 volts in 10 millivolt steps. (Continued)

Program for the HP 9830 (BASIC Language) (Continued).

Program	Remarks
1020 CMD "?U!"	
1030 OUTPUT (13,*)"A",A,"I"	Send amplitude value to 172B. This is done by sending first the ASCII letter A, then the amplitude in variable A, followed by the letter I which causes the Execute action, that transfers the information programmed since the last Execute was sent to the waveform generator circuits.
1040 NEXT I	Increment A by 10 millivolts and test if 11 volts have been reached.
1050 STOP	Stop program.

Example 2. Testing SRQ bit, polling and reading error message from the 172B.

Program for the HP 9825 (using the rds function)

0: dim E$ [50]	
1: wrt 701,"C30"	Cause an error in the 172B so that it will request service.
2: if bit (7,rds (7));gto 5	Wait at statement 2 until SRQ comes on.
3: dsp "SRQ NOT ON"	
4: gto 2	
5: dsp "SRQ ON"	
6: wrt 701, "T1"	Set 172B Talk message response setting to select the error message. It is necessary to do this before polling because the 9825 polling function sends the instrument talk address before the Serial Poll Enable (SPE) command. Thus, the 172B sees itself briefly addressed as a talker and fetches the selected talk message at that time.
7: rds (701) → A	Poll 172B and put its status byte in the variable A.
8: if A = 69 gto 10	Test if correct status byte (69 = decimal equivalent of ASCII letter E).
9: dsp "BAD STATUS BYTE";stp	If not, status byte is bad.
10: red 701, E$	Read error string into the string variable E$.
11: dsp E$	Display error string. Should look like E 1 C.
12: stp	

Table C-1. 172B Programming Examples (Continued)

Example 2. Testing SRQ bit, polling and reading error message from the 172B. (Continued)

Program for the HP 9830.

Program	Remarks
1000 DIM E$ [50]	
1010 CMD "?U!","C30C"	Cause an error in the 172B so that it will request service.
1020 IF STAT13< =0 THEN 1050	Wait at statement 1020 until SRQ comes on.
1030 DISP "SRQ NOT ON"	
1040 GO TO 1020	
1050 DISP "SRQ ON"	
1060 CMD "?U"	Set up calculator to talk for sending commands.
1070 FORMAT 5B	Binary format for sending commands.
1080 OUTPUT (13,1070)256,95,53,24, 65,512	Perform the following: turn on ATN line; send UNTALK command; send calculator listen address (so calculator can receive status byte); send Serial Poll Enable (SPE) command; send 172B's talk address, which commands it to send the status byte to the calculator; finally, turn off ATN. Note that the 172B's talk address is sent after the SPE command; this ensures that the instrument will not try to access a talk message during a poll.
1090 A=RBYTE13	Poll 172B and put its status byte in the variable A.
1100 IF A=69 THEN 1130	Test if correct status byte (69 = decimal equivalent of ASCII letter E).
1120 STOP	
1130 OUTPUT (13,1070)256,95,25,512	Finish poll by unaddressing 172B (with 95) and sending a Serial Poll Disable command (25).
1140 CMD "?5A"	Address 172B to talk and calculator to listen.
1150 ENTER (13,*) E$	Read error string into the string variable E$.
1160 DISP E$	Display error string. Should look like E 1 C.
1170 STOP	

Table C-1. 172B Programming Examples (Continued)

Example 3. Reading Contents of Stored Settings Into Calculator.

Program for the HP 9825.

Program	Remarks
0: dim S$ [80]	
1: wrt 701,"T0Q1Y",A	Initialize: Select talk response zero, which reports back a condensed reading of amplitude, offset, frequency, mode, function, load and symmetry. Also, enable GPIB Service Request (SRQ) for errors and recall the stored setting selected by the value in the variable A, which has previously been set to the lowest numbered setting to be read.
2: red 701, S$	Read program information just recalled into the variable S$.
3: wrt 701,"W"	Command 172B to advance to and recall next program.
4: (instructions to save S$ on tape or other storage)	
5: wait (100)	Insure that 100 ms have elapsed since the "W" was sent to allow time for the SRQ to be valid. This statement may be unnecessary if statement 4 lasts longer than 100 ms.
6: if not bit (7, rds (7));gto 2	Test if SRQ line is on. If not, go to statement 2 and read next program. If on, the last setting has been read.

Program for the HP 9830.

1000 DIM S$ (80)	
1010 CMD "?U!","T0Q1Y"	Initialize: Select talk response zero, which reports back a condensed reading of amplitude, offset, frequency, mode, function, load and symmetry. Also, enable GPIB Service Request (SRQ) for errors and recall the stored setting selected by the value in the variable A, which has previously been set to the lowest numbered setting to be read.
1020 OUTPUT (13,*) A	
1030 CMD "?A5"	Address 172B to talk and 9830 to listen.
1040 ENTER (13,*) S$	Read program information just recalled into the variable S$.
1050 CMD "?U!","W"	Command 172B to advance to and recall next program.
1060 (instructions to save S$ on tape or other storage)	

Table C-1. 172B Programming Examples (Continued)

Example 3. Reading Contents of Stored Settings Into Calculator (Continued)

Program for the HP 9830 (Continued).

Program	Remarks
1070 WAIT (100)	Insure that 100 ms have elapsed since the "W" was sent to allow time for the SRQ to be valid. This statement may be unnecessary if statement 1060 lasts longer than 100 ms.
1080 IF STAT13>1 THEN 1040	Test if SRQ line is on. If not, go to statement 1040 and read next program. If on, the last setting has been read.

Example 4. Logarithmic frequency sweep using high speed recall of stored settings.

Program for the HP 9825.

0: wrt 701,"A1D0B0C0P1S0"	Initialize settings to produce a 1 volt continuous sine wave.
1: for I = 1 to 240	Generate 240 settings with frequency logarithmically spaced between 1 kHz and 1 MHz.
2: (I − 1)/80 + 3→E	Compute exponent of next frequency.
3: wrt 701,"F",10↑E,"M",I	Send new frequency to instrument and store into the program selected by I.
4: next I	
5: wrt 701,"Y1"	Recall first program to begin sweep.
6: "LOOP": wrt 701,"O1"	Program the 172B to fetch the next stored program when a Group Execute Trigger is sent to it.
7: for I = 1 to 239	Send 239 GETs to the 172B to fetch and execute the stored programs numbered 2 through 240, which will sweep the output frequency from 1 kHz to 1 MHz.
8: trg 701	
9: next I	
10: wrt 701,"O − 1"	Program the 172B to fetch the previous stored program when a Group Execute Trigger is sent to it.
11: for I = 1 to 239	Send 239 GETs to the 172B to fetch and execute the stored programs numbered 239 through 1 in descending order, which will sweep the frequency from 1 MHz to 1 kHz.
12: trg 701	

Table C-1. 172B Programming Examples (Continued)

Example 4. Logarithmic frequency sweep using high speed recall of stored settings. (Continued)

Program for the HP 9825 (Continued).

Program	Remarks
13: next I	
14: gto "LOOP"	

Program for the HP 9830

1000 CMD "?U!","A1D0B0C0P1S0"	Initialize settings to produce a 1 volt continuous sine wave.
1010 FOR I = 1 TO 240	Generate 240 settings with frequencies logarithmically spaced between 1 kHz and 1 MHz.
1020 E = (I−1)/80+3	Compute exponent of next frequency.
1030 CMD "?U!"	
1040 OUTPUT (13,*)"F",10↑E,"M",I	Send new frequency to instrument and store it into the program selected by I.
1050 NEXT I	
1060 CMD "?U!","Y1"	Recall first program to begin sweep.
1070 CMD "?U!","O1"	Program the 172B to fetch the next stored program when Group Execute Trigger is sent to it.
1080 FOR I = 1 TO 239	Send 239 GETs to the 172B to fetch and execute the stored programs numbered 2 through 240, which will sweep the output frequency from 1 kHz to 1 MHz.
1090 OUTPUT (13,1100)256,8,512;	
1100 FORMAT 3B	
1110 NEXT I	
1120 CMD "?U!","O−1"	Program the 172B to fetch the previous stored program when a Group Execute Trigger is sent to it.
1130 FOR I = 1 TO 239	Send 239 GETs to the 172B to fetch and execute the stored programs numbered 239 to 1 in descending order, which will sweep the frequency from 1 MHz to 1 kHz.
1140 OUTPUT (13,1100)256,8,512;	
1150 NEXT I	
1160 GO TO 1070	